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**Fabrication of a CMOS compatible nanopore detector for DNA** ASHFAQUE UDDIN, KAVEH MILANINIA, Dept. of Electrical & Computer Eng., UCSB, OGUZ ELIBOL, JONATHAN DANIELS, XING SU, MADOO VARMA, Integrated Biosystems Lab, Intel Corp., DEREK STEIN, Dept. of Physics, Brown University, LUKE THEOGARAJAN, Dept. of Electrical & Computer Eng., UCSB — Nanopore based DNA sequencers require integration of miniaturized electrodes and amplifier electronics in close proximity to the nanopores in a CMOS platform. This will facilitate portability, enable faster analysis, and improve sensing performance. Here we report for the first time the fabrication of a DNA nanopore detector compatible with a standard CMOS process. Our nanopore devices are made using an N+ polysilicon/gate oxide/N+ polysilicon stack on an oxidized silicon substrate identical to the AMI  $0.5\mu$  process. The nanopores are created in the gate oxide membrane (36 nm) while doped polysilicon layers (250 and 370 nm) act as electrodes to apply bias across pores. Five lithography masks are used to pattern the oxide membrane and the electrodes. The nanopores are defined by etching the membrane using electron beam lithography patterned holes in a resist mask. Using this method we have directly fabricated pores with diameters as small as 11 nm, without applying conventional pore shrinkage techniques. This is enhanced by cold development of the e-beam exposed resist resulting in sub-10 nm pores. DNA experiments are currently underway utilizing our nanopores.

Prefer Oral Session  
 Prefer Poster Session

Ashfaq Uddin  
ashfaq@ece.ucsb.edu  
Dept. of Electrical & Computer Eng., UCSB

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