

A $1.3\mu W$ $0.0075mm^2$ Neural Amplifier and Capacitor-Integrated Electrodes for High Density Neural Implant Recording

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Abstract—A key issue in the design of biomedical implants is the design of low-power area-efficient circuits that allow for high-density neural recording. This paper presents an ultra low-power ($<1.4\mu W$), area efficient low-noise neural amplifier that utilizes current-feedback miller-compensation technique and occupies $<0.08mm^2$ silicon area. Integrating the large input capacitor within the electrodes saves valuable silicon area. The amplified signal is digitized by a 10-bit sigma-delta ADC that is based on an area-efficient self-biased amplifier. The ADC consumes only $4.8\mu W$ from a $1.2V$ supply, when sampled with a $1.6MHz$, and occupies $0.03mm^2$ chip area. The chip was fabricated in $0.13\mu m$ CMOS.

I. INTRODUCTION

The exponential advances in microfabrication coupled with our increased understanding of neural diseases enable designing highly sophisticated novel devices that benefit patients suffering from neurodegenerative diseases. In these diseases, it is not enough to just stimulate, it is also essential to record from the brain to effectively complete the feedback-loop that is absent due to a disease or trauma. Thus, by recording signals from the brain, patients were able to control the environment around them thereby enhancing their quality of life [1].

Typically, it is common to record from a larger population of neurons while stimulating a few. For example, the state of the art stimulation device, which impressively restores partial hearing, is the cochlear implant which possesses only 21 electrodes [2]. For recording, on the other hand, it has been shown that the ability to guide a robotic arm to a limited number of targets in 2-D and 3-D can be implemented with tens of neurons [3], while recording devices with higher accuracy requires recording from several hundreds of neurons [4]. Therefore to effectively map the neural code it would be ideal to record from several hundreds to even thousands of neurons. This additional scale of the problem brings unique challenges to the design of the implant, one that necessitates the design of low-power area-efficient circuits.

Neural action potentials occupy frequencies ranging from $100Hz - 6KHz$ and have amplitudes on the order of $50 - 1000\mu V$ and thus require amplification via a neural low noise amplifier (LNA). Faradic reactions at the electrode-tissue interface can lead to large DC offsets that can be as high as few volts [5]. To prevent saturating the neural amplifier, the

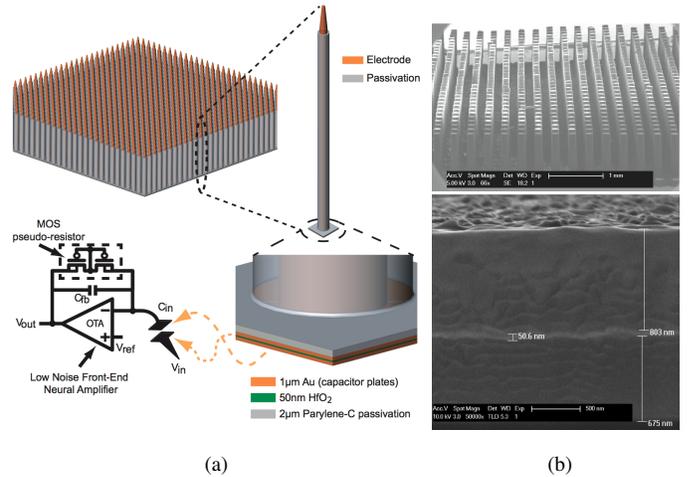


Fig. 1. (a) Low-noise frontend neural amplifier and the capacitor-integrated electrodes. Each electrode integrates C_{in} within itself and thus significantly reduces the silicon area required per neural amplifier. (b) (Top) SEM of a micromachined polymer (PDMS) 32×32 electrode array coated with gold, (Bottom) SEM image of the cross-section of the parallel plate capacitor showing the $50nm$ HfO_2 deposited using ALD.

recorded signal is usually AC-coupled to the LNA and the mid-band closed-loop gain is set by the ratio of C_{in} to the feedback capacitance, C_{fb} . However, higher gain in the LNA require a larger capacitance ratio, which means larger silicon area per amplifier as C_{in} dominates the area. As shown in figure 1a, integrating the input capacitance as parallel plate capacitor with the recording electrodes can provide significant silicon area saving and allows for high-density neural implant recording. This is the first time in the literature to attempt integrating the capacitor into the neural recording electrodes. Figure 1b shows our recent efforts in microfabricating a polymeric neural electrode array that has been metalized with gold. Preliminary measurement of the HfO_2 based capacitors fabricated using atomic layer deposition, ALD, shows that the capacitance variation is minimal and the obtained density is $4fF/\mu m^2$, which is comparable to that of dual-MIM capacitors available on-chip. Further work is ongoing to integrate C_{in} with the electrodes and interface them with the chip, but currently in this paper the recording was performed with on-chip MIM capacitor. We expect to integrate the electrode array with the

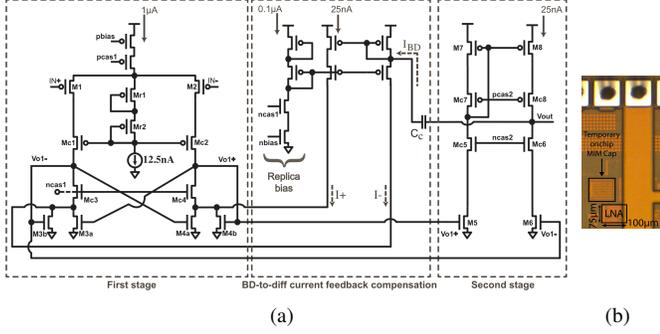


Fig. 2. (a) Schematic of the OTA used in the neural amplifier, (b) die photo showing the LNA and the temporary on-chip MIM capacitor. A transistor-only bias network as in [10] is used and is not shown here.

CMOS chip and show the results in a subsequent publication in the near future. Once the neural data is amplified, it is digitized by a low-power area-efficient 10-bit sigma-delta analog-to-digital converter (ADC) based on a self-biased amplifier [6].

This paper is organized as follows. Section II describes the operation of our low-power, low-noise, area-efficient neural amplifier that relies on capacitor-integrated electrodes. Section III presents its simulation and measurement results. Section IV shows measurement of neural action potentials using our neural amplifier and the low-power sigma-delta ADC based on a self-biased amplifier. Section V concludes the paper.

II. LOW-POWER LOW-NOISE AREA-EFFICIENT NEURAL AMPLIFIER

The low-noise amplifier was designed under strict power, area, and noise constraints as discussed in our prior publication [7]. The maximum power consumption for a brain implant is 10 mW as cells would die if exposed to elevated temperatures for extended periods of time. For a 1024 channel implant, the LNA power budget is thus restricted to 2 \$\mu\$W. The area of the CMOS chip should be minimized, for yield and cost reasons. For a chip area of 4x4 mm², the total LNA area/channel should be restricted to no more than 0.01 mm² to leave for the ADC conversion and the wireless transmission.

A. Neural Amplifier with Capacitor-Integrated Electrodes

The neural amplifier shown in figure 1a The values of C_{in} and C_{fb} are 20 pF and 0.2 pF respectively for a nominal gain of 40 dB. DC feedback is accomplished by two symmetrical back-to-back diodes acting as a MOS pseudo-resistor that realizes very large small-signal impedance [8]. Together with C_{fb} , it introduces a low frequency pole at frequency <100 Hz and it provides larger resistance than the topology in [9] for large input-output voltage difference. Since the large C_{in} is integrated into the recording electrodes, as shown in figure 1a, huge area savings per channel is achieved. V_{ref} is the reference voltage to which all node voltages and measurements are referred with respect to, and it is connected to the supply's mid-rail, through the use of two half-wave rectifiers [10].

B. Neural Amplifier OTA's Architecture

In figure 2a the first stage's active load consists of cascoded cross-coupled pair and diode-connected devices. This technique embeds the common-mode feedback (CMFB) circuit into the first stage and no external CMFB is required [11]; thus saving power. It also achieves a very low common mode load-resistance and thus improves the common mode rejection ratio, CMRR, as well. It can be shown that active load's differential resistance, R_{Ld} , is given by:

$$R_{Ld} \simeq 2 \frac{g_{mc3} r_{oc3} r_{o3,eff}}{1 + (g_{m3b} - g_{m3a}) g_{mc3} r_{oc3} r_{o3,eff}} \quad (1)$$

where r_{o3} , and r_{oc3} are the intrinsic output resistances of the load and cascode NMOS devices respectively.

Equation (1) shows that large resistance in differential mode can be realized. Even if negative differential R_{Ld} resistance, due to transistor mismatch, occurs, the overall first stage's output resistance is still positive because R_{Ld} is much larger than the resistance looking into the drain of the PMOS devices.

The OTA's compensation is done through current feedback. The current is converted into a differential signal via a bidirectional-to-differential current converter [12], and then fed into the first stage. Using this approach and with the high gain in the cascoded second stage, a small compensation capacitor ($C_c = 1$ pF) is needed to provide a unity gain frequency of 1 MHz and phase margin around 50°. This is another area saving even when compared to other architectures that use single stage operational transconductance amplifier, OTA, and a bandwidth limiting load capacitance, C_L [9], [13].

In the proposed OTA 91% of the total power is used in the first stage (the replica bias circuit is shared between several OTAs). The current in the second stage was designed to drive C_{fb} and the input sampling-capacitor of the following sigma-delta ADC while providing enough slew-rate for the largest expected signal swing at the highest frequency.

All transistors are operating in subthreshold in saturation. Thus the current shot-noise power is given by [14]:

$$\overline{i_n^2} = 2qI\Delta f \quad (2)$$

where, I is the DC current flowing through the transistor, and Δf is the noise bandwidth in Hz.

The current in the OTA's first stage was designed to minimize its shot-noise to be able to detect the minimum expected neural activity within the allowed power budget. The transistor's input-referred noise voltage power is given by:

$$g_m = \frac{qI}{nkT} \Rightarrow \overline{v_{n,in}^2} = \frac{2 \cdot (nkT)^2}{qI} \Delta f \quad (3)$$

where n is the subthreshold slope factor, k is the Boltzmann constant, T is the temperature in Kelvin, and the theoretical transconductance, g_m , in subthreshold was used.

III. OTA'S SIMULATIONS AND MEASUREMENTS

The amplifier was designed and fabricated in 0.13 \$\mu\$ m CMOS technology. The simulated current consumed by a single OTA is 1.1 \$\mu\$A from a 1.2 V supply. The amplifier's

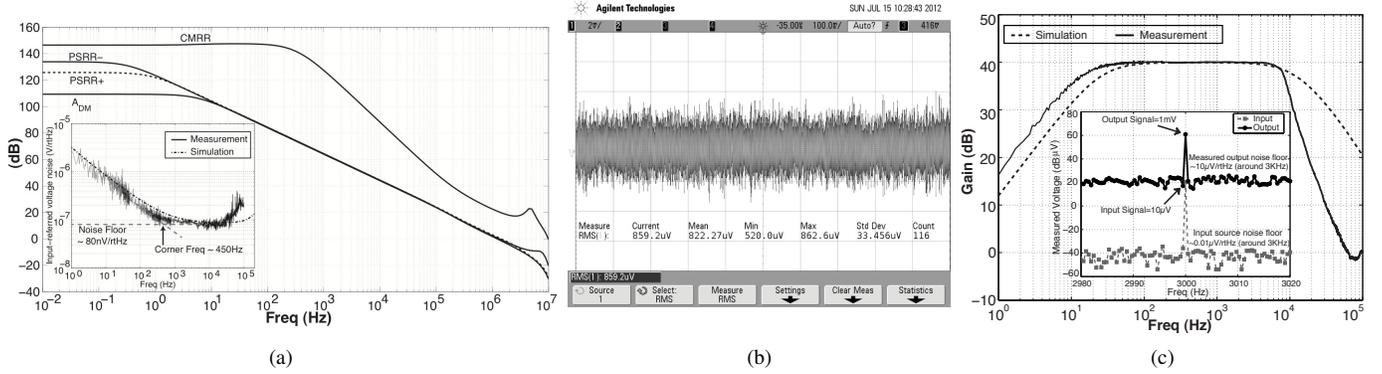


Fig. 3. (a) Simulated open loop A_{DM} , CMRR, PSRR, PSRR. Inset: Measured and simulated (dashed-lines) input-referred noise PSD. (b) RMS noise is $8.22\mu V$ when referred to the input. (c) Simulated and measured gain of the neural amplifier. frequency roll-off is faster due to a second order 10-KHz low pass filter that was placed at the pads for measurements reasons. It seems that there was a shift in the LPF cut-off which makes the BW of the neural amplifier appear to be 8KHz. Inset: Measured output (top trace) for a $10\mu V$ input (bottom trace) at 3KHz.

area is $\sim 0.0075mm^2$ as shown in the die photo in figure 2b. Figure 3a shows simulation results indicating DC open loop differential mode gain, A_{DM} , of $109dB$, a DC common mode rejection ratio, CMRR, of $146dB$, and DC power supply rejection ratios (PSRR+, PSRR-) of $125dB$ and $133dB$ from the positive and negative supply rails respectively. Thanks for the cross-coupled pair and subthreshold operation.

The OTA's theoretical input-referred shot-noise voltage is:

$$\overline{v_{n,in}} = \frac{\sqrt{i_{n,1}^2 + i_{n,2}^2 + i_{n,3a}^2 + i_{n,3b}^2 + i_{n,4a}^2 + i_{n,4b}^2}}{g_{m1,2}} \sqrt{\Delta f} \quad (4)$$

where $i_{n,i}^2$ is the current noise-power in transistor M_i , and $g_{m1,2}$ is the transconductance of the input differential pair. Since the DC current through $M_{3,4}$ is half that of $M_{1,2}$, therefore $\overline{v_{n,in}} = 71.2nV/\sqrt{Hz}$.

The amplifier's simulated and measured input-referred noise voltage PSD is shown in the inset of figure 3a. The post-layout simulated shot-noise floor is $88nV/\sqrt{Hz}$ for frequencies $>2KHz$, while the measured is $\sim 80nV/\sqrt{Hz}$. This is very close to the theoretical calculation above, which does not take into account all the devices. Figure 3b shows a total rms noise of $8.22\mu V$ when referred to the input.

Figure 3c shows the simulated vs. measured closed loop gain. All measurements were done using SR770 Network Analyzer on battery-powered chips. The smaller BW is due to an estimated $1pF$ package capacitance that will be buffered correctly for measurement purposes in the next chip. The inset in figure 3c shows the measured output spectrum for a $10\mu V$ input sinusoid at $3KHz$. The measured output noise floor around $3KHz$ is about $\sim 10\mu V/\sqrt{Hz}$, which translates to $\sim 100nV/\sqrt{Hz}$ when referred to the input and matches the measured input-referred noise trace in the inset of figure 3a. Notice that in our measurement setup, the source's input noise is very low and thus the output noise is dominated completely by our amplifier's noise as can be seen in the inset of figure 3c. However, in a recording environment, and if recording with an electrode whose resistance were $1M\Omega$ operating at in-vivo temperature and with $10KHz$ recording bandwidth, the rms thermal noise voltage would be around $12.9\mu V_{rms}$, which is

higher than our amplifier's total input integrated noise. The noise efficiency factor, NEF of the amplifier is $3.8(3.3)$ for a BW of $8KHz(10KHz)$ corresponding to the measured BW and the actual BW without the extra parasitic pad capacitance. However, a better metric is the one that includes power and area into account ($NEF^2 * Volt * Area$) and it evaluates to 0.1 for our amplifier; which is much less, to the best of our knowledge, than all other amplifiers that exist in the literature in CMOS technology.

The OTA's current consumption measured across 20 chips is $\sim 1.1\mu A$ with a standard deviation of $0.2\mu A$. Table I compares this work with other work in the literature. Among all CMOS amplifiers in the table that operate in the same frequency band, our amplifier dissipates the lowest power and occupies the smallest area while achieving similar NEF.

IV. NEURAL ACTION POTENTIALS MEASUREMENT

In our measurement setup we used the neural action potentials data that have been collected from two male macaques performing a visual oddball discrimination paradigm [18]. The data were loaded into Agilent's 33522A arbitrary function generator, attenuated with a 50X attenuator and then fed to the neural amplifier. The amplitude of the overall data set was

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER WORK

Reference	[9]	[15]	[16]	[17]	This work
Tech. (μm)	1.5	0.18	0.25	0.13	0.13
Gain (dB)	39.5	40	40.4	40.5	40
VDD (V)	± 2.5	1.8	0.9	1	1.2
Current (μA)	16	3(11.1)	1.1	12.5	1.1
BW (Hz)	25m-7.2k	350-11.7k	30-8.9k	0.4-8.5k	10-10k
$V_{ni,rms}$ (μV)	2.2	11.2(5.4)*	6.76	3.2	8.2
NEF	4.0	5.9(4.4)	2.92	4.5	3.3(3.8) [†]
Area (mm^2)	0.16	0.03	0.05	0.047	0.0075
NEF ² .V.A	12.8	1.88(1.05)	0.38	0.95	0.1(0.12)

* Total integrated IRN from 10Hz to 65KHz. Reported values correspond to lowest(highest) current setting.

[†] Measured BW was 8KHz due to an estimated 1pF that wasn't buffered correctly. Values correspond to 8(10)KHz BW.

collectively scaled to test the limit of detection. The spikes before the attenuator and those at the output of the neural amplifier are shown in figure 4a as observed on Tektronix's TPS2014B oscilloscope. The largest spike's amplitude, when referred to the input, is about $150\mu V_{pp}$, while the smallest is about $80\mu V_{pp}$. It was not possible to show $10\mu V_{pp}$ spikes on the oscilloscope due to its limited resolution of $2mV/div$.

In another measurement setup, the amplifier's output was digitized by a low-power 10-bit sigma-delta ADC using a sampling frequency of $1.6MHz$. Since the neural amplifier is single-ended output due to the constraints imposed by capacitor-integrated recording electrodes, the negative input terminal of the ADC is tied to V_{ref} . We chose to use fully differential ADC architecture in our design as it allows for a robust self-biased amplifier design, and to reduce common-mode noise injection to the signal path due to the many switching events in the switched capacitors in the sigma-delta ADC. The sigma-delta stream was transferred to a PC using Agilent MSO71404B mixed signal scope for digital processing using Matlab and Simulink. The reconstructed neural action potentials data is shown in figure 4b after digitally removing the high frequency noise using a sinc³ filter. The largest spike's amplitude, when referred to the input, is about $500\mu V_{pp}$, which corresponds to the maximum neural signal we expect to record. The neural data were reconstructed properly without any significant distortion to the spikes' shapes.

V. CONCLUSION

We have presented in this paper the design of another ultra low-power and area-efficient building block for neural recording systems. The proposed current-mode miller feedback low-noise neural amplifier consumes $<1.4\mu W$ of power while occupying an area $\sim 0.0075mm^2$. We proposed our novel approach of integrating the input capacitor within the electrodes to save precious silicon area. We successfully digitized the data with a low-power 10-bit sigma-delta ADC that is based on an area-efficient self-biased amplifier which consumes only $4.8\mu W$, while occupying an area of $0.03mm^2$. Such low-power area-efficient circuits are the key to building high-density neural implants that can support an excess of several hundred electrodes. We have shown the measurement results of neural action potentials that were previously recorded from two male macaques performing a visual oddball discrimination paradigm. We were able to successfully reconstruct the neural action potentials data that was amplified by the neural amplifier and then digitized through our ADC. Ongoing work in our lab is currently focusing on the development of the capacitor-integrated electrodes and interfacing them with the CMOS chip.

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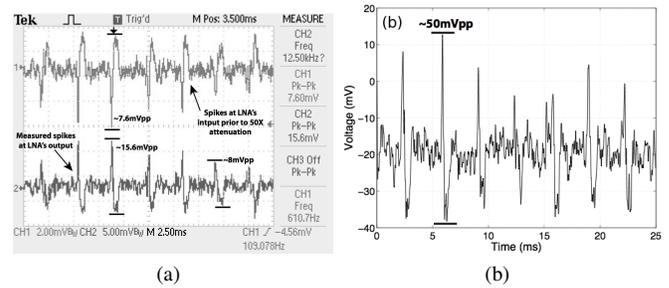


Fig. 4. (a) Neural action potentials recorded using our neural amplifier. Top curve (CH1) is the input (prior to 50X attenuation). Bottom curve (CH2) is the output from the 100X gain neural amplifier. (b) Reconstructed neural action potentials at the sigma delta ADC output after digitally removing the high-frequency noise using a sinc³ filter.

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