Wafer Scale Integration of CMOS Chips for Biomedical Applications via Self-Aligned Masking

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***Abstract*— This paper presents a novel technique for the integration of small complementary metal-oxide semiconductor (CMOS) chips into a large area substrate. A key component of the technique is the CMOS chip-based self-aligned masking. This allows for the fabrication of sockets in wafers that are at most 5 μm larger than the chip on each side. The chip and the large area substrate are bonded onto a carrier such that the top surfaces of the two components are flush. The unique features of this technique enable the integration of macroscale components, such as leads and microfluidics. Furthermore, the integration process allows for microelectromechanical systems micromachining after CMOS die-wafer integration. To demonstrate the capabilities of the proposed technology, a low-power integrated potentiostat chip for biosensing implemented in the AMI Semiconductor's 0.5 μm CMOS technology is integrated in a silicon substrate. The horizontal gap and the vertical displacement between the chip and the large area substrate measured after the integration were 4 and 0.5 μm, respectively. A number of 104 interconnects are patterned with high-precision alignment. Electrical measurements have shown that the functionality of the chip is not affected by the integration process. A CMOS/microfluidic hybrid system is also demonstrated based on the proposed integration technology.**

***Index Terms*— Benzocyclobutene, bonding, chip-specific integration, complementary metal-oxide semiconductor, interconnect, microelectromechanical systems, packaging, planarization, spin-on-glass.**

I. Introduction

THE integration of microfluidics, microelectromechanical systems (MEMS) and electronics within a compact footprint can revolutionize the area of handheld sensors for bio-threat detection and personalized medicine. Furthermore, this integration has the potential to deliver new types of instrumentation that can enable the discovery of new physics at the nanoscale, thanks to the vast parallelism afforded by lithographic integration. The major hurdle in realizing this vision has been the co-integration of complementary metal-oxide semiconductor (CMOS) devices with sensors, actuators, and microfluidics due to either incompatibility of scale or processing conditions.

Another important consideration in integrated biomedical devices is the cointegration of passive components for signal conditioning or the integration of heterogeneous die in the case of optoelectronic platforms. Unlike transistors, passive devices such as capacitors and inductors do not scale well, and can occupy valuable silicon real-estate raising die costs and lowering the yield. Furthermore, radio frequency (RF) devices require careful tuning of passive characteristics that can often enable superior performance. By using a post-integration methodology, passive components can be integrated without the associated package parasitics.

Traditionally, packaging and interconnection of disparate chips are performed by laborious and expensive techniques such as wire, flipchip, and tape-automated bonding [1]. The density of interconnects that can be achieved with these techniques is limited. To accomplish high-resolution and high-density integration, several system-in-package (SIP) methods have been proposed in the past few years. For example, high-density interconnect (HDI) technology by general electric [1], [2], chip-level integrated interconnect (CL-I^2) technology by Rodger *et al.* [3], [4], bumpless build-up layer (BBUL) packaging by Intel [5] and self-aligned wafer-level integration technology (SAWLIT) by Sharifi *et al.* [6]. All these technologies share a similar protocol for the integration of chips. First, chips are embedded in etched cavities in a carrier substrate. A passivation layer is then created on top of chips and carrier using a polymer material. At the end, chip-to-package interconnections are patterned by applying photolithography and metal etching or lift-off. However, none of the proposed technologies offers the formidable combination of microfluidic integration and post-CMOS micromachining of the packaged CMOS circuitry. Furthermore, these technologies can suffer from low yield, poor die-to-die alignment accuracy and lack of robustness.

We present here for the first time a versatile chip-specific integration technology (VCSIT) which is CMOS, MEMS and bio-compatible, and offers both robustness and very accurate alignment. By judicious choice of materials we have designed a platform that can easily support post-CMOS micromachining. We introduce a self-aligned process that enables a robust integration of the die and the wafer. Furthermore, our process can be easily extended to integrate multiple dies on the same wafer. This gives an alternative approach to 3-D-integration for

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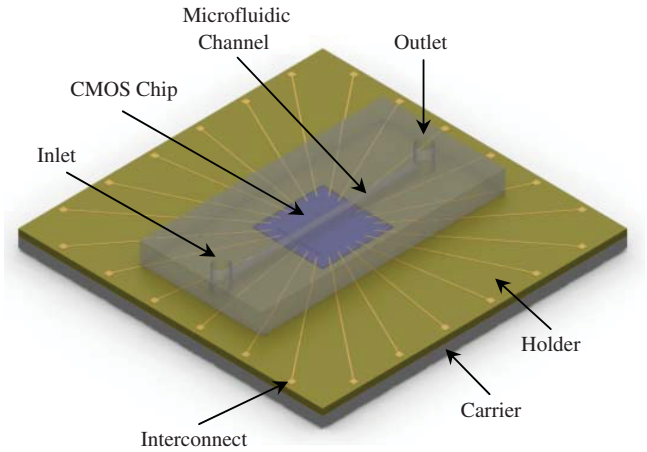


Fig. 1. Envisioned fully integrated biochip utilizing VCSIT.

integrating logic and memory components in close proximity, while simultaneously mitigating heat dissipation issues that remain a problem for 3-D integration [7], [**?**].

This paper is organized as follows. We first give a detailed description of our integration process using a foundry-fabricated CMOS chip in Section II. We then evaluate the electrical performance of the packaged chip in Section III. The advantages and capacity of our proposed packaging technology are elucidated in Section IV. We then summarize our contribution and discuss some future work in Section V.

II. VCSIT

To demonstrate VCSIT, we used a CMOS chip, which is a low-power integrated potentiostat for biosensing, implemented in the AMI Semiconductor's 0.5 μm technology. It is 3 mm $\times$ 3 mm $\times$ 260 μm in dimension, fabricated via the MOSIS. The chip is integrated using two silicon substrates referred to as *holder* and *carrier* (Fig. 1). The holder serves as the housing for the chip. The holder and the chip are bonded onto a carrier by adhesive bonding using benzocyclobutene (BCB). The top surface of the bonded chip and substrate is planarized by applying spin-on-glass (SOG). Interconnects leading from the chip to the holder are then patterned via a lift-off process. The schematic of a fully integrated biochip implemented using VCSIT is given in Fig. 1. The VCSIT process is elaborated in the following sub-sections.

A. Chip Specific Cavity

The first step in the integration process is to create a cavity in a silicon holder where the CMOS chip will fit tightly. Chips obtained from different foundries can often vary in size by as much as 10–50 μm due to the thickness variation of the dicing saw that is used to dice the chips [6]. Hence, a single-size photomask cannot accommodate holes in the holder which are only a few micrometers larger on each side than individual chips. To resolve this issue, a chip-based lithography was implemented where individual chips are used as masks for photolithography to pattern holes.

The process starts with the thermal oxidation (oxide thickness $\sim$2 μm) of a 260 μm thick silicon wafer. The oxidized wafer is coated with the negative photoresist, AZ5214. A hole with the same size as the chip is then patterned in the resist by placing the chip on the resist-coated wafer, and using it as photomask [Fig. 2(a) and (b)]. The pattern is then transferred to the oxide layer by an inductively coupled plasma (ICP) etch. Using the patterened oxide as a mask, a through-wafer hole is etched by a deep reactive ion etch (DRIE) Bosch process [Fig. 2(c)]. At the end, the oxide layer is removed by buffered hydrofluoric acid [Fig. 2(d)]. Fig. 3 shows a microscopic top-view after the CMOS chip is placed inside the holder. The placement of the chip was done with the help of a flip-chip bonder. The gap between the holder and the chip was measured to be 4 μm.

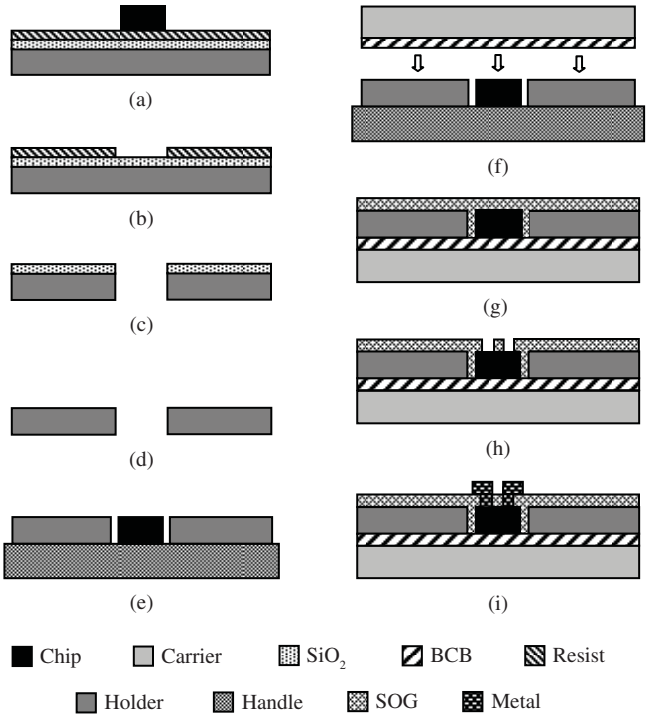


Fig. 2. VCSIT process steps to package a chip. (a) Chip is placed on the resist-coated, oxidized silicon holder. (b) Hole with the same size as the chip is patterned in the resist using the chip as photomask. (c) Pattern is transferred to the oxide layer, and through-holder etch is performed. (d) Oxide on the holder is removed. (e) Holder and the chip are placed face-down on a handle substrate. (f) BCB-coated carrier is bonded with the backside of the chip and the holder. (g) Gap between the chip and the holder is filled and the top surface is planarized with SOG. (h) Vias to the contact pads of the chip are created. (i) Metal interconnects from the chip to the holder are patterned.

B. Bonding

The second part of the integration process involves bonding the chip and the holder onto a carrier wafer. The carrier provides strong support and robustness to the packaged chip. Chips obtained from MOSIS usually have a rough surface on the backside due to back-grinding. Adhesive bonding is chosen for the bonding of holder and chip onto the carrier, since it requires no special substrate surface treatments such as planarization, chemical modifications, etc. In addition, adhesive bonding is robust, low-temperature, low-cost, and able to join heterogeneous substrates [8], [9].

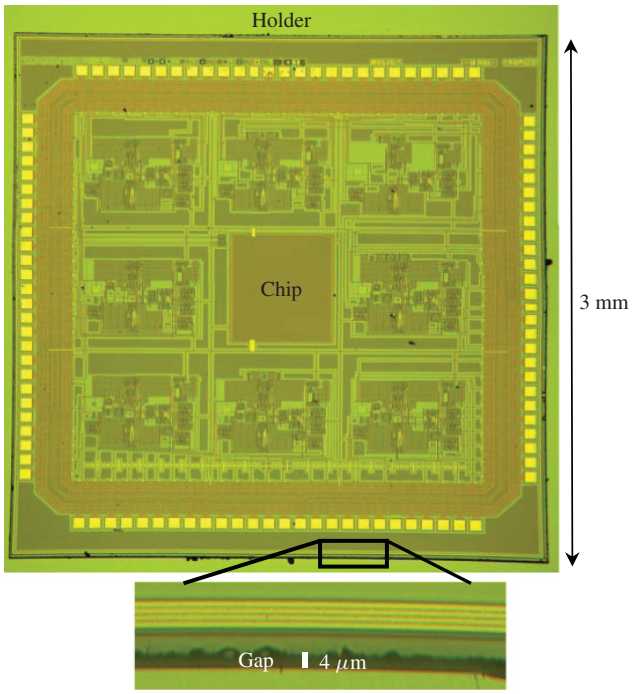


Fig. 3. Top-view of a CMOS die placed inside holder.

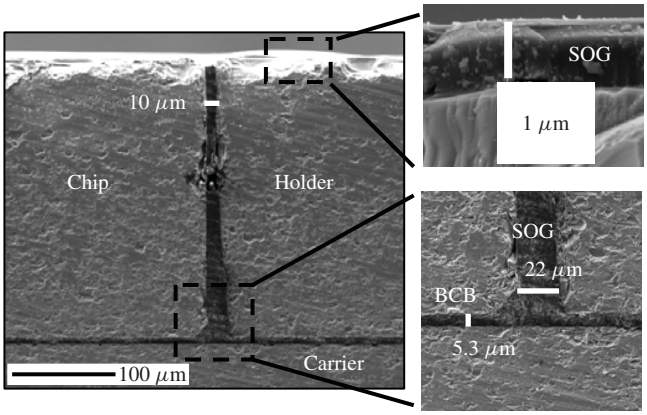


Fig. 4. SEM cross-section of a packaged chip.

Various materials are available to use as adhesives, e.g., BCB, SU8, polydimethylsiloxane (PDMS), polyimide, etc. The choice of a suitable adhesive for bonding is primarily based upon thermal and mechanical stability, and chemical resistance to acids, bases or solvents to which it may be exposed to during subsequent fabrication processes. We chose BCB as the adhesive, since it offers a very high bond strength and excellent resistance to a number of strong chemicals. BCB is also known to be CMOS, MEMS, and bio-compatible [8]–[10].

The bonding process starts with coating of the adhesion promoter, AP3000, on the carrier. This is followed by the spin-coating of a 7-μm thick layer of photosensitive BCB (Cyclotene 4024-40, Dow Chemical Company). BCB is pre-cured at 100 °C for 90 s. The precuring step prevents void formation from trapped air and out-gassing of solvent at the bond interface [8]. The holder and the chip are then positioned face-down on a handle wafer [Fig. 2(e)]. The backside of the chip and the holder are coated with AP3000. The BCB-coated carrier is then flipped, and placed on the backside of the holder and the chip [Fig. 2(f)]. The surfaces are bonded under pressure at elevated temperature in a Karl Suss SB-6 wafer bonder. The BCB carrier–holder interface is fully cured at 250 °C in N_2 ambient for an hour. A slow temperature ramp of about 1.5 °C/min is used to reach the curing temperature of 250 °C to reduce stress in the film.

The strength of the BCB bond is tested by harsh ultrasonic agitation, and further by cutting with a dicing saw. No delamination of the bonding interface has been observed.

C. Gap Filling and Planarization

In this part of the integration, the top surfaces of the chip and the holder are planarized in order to have a seamless transition from the chip to the holder. This is crucial for subsequent process steps such as patterning contacts from perimeter pads of the chip to the remote pads on the holder. Any discontinuity at the chip–holder interface will lead to broken metal lines and, thus, open circuits.

The critical aspect of the planarization step is to fill and bridge the high-aspect-ratio (HAR) gaps between the chip and the holder. High density plasma chemical vapor deposition of oxide has been the preferred method to fill gaps with aspect-ratios around 3. However, as the aspect-ratio increases, reliable gap-filling becomes increasingly difficult due to the void formation during the gap-filling process [12], [13]. A void-free and cost-effective method to fill HAR gaps is by using SOG. Because of its low viscosity, SOG can easily reach the bottom of the narrow and HAR gaps, and completely fill them without voids while planarizing the surface [11], [14]. Hence, SOG (Accuglass 512B by Honeywell, Inc.) is chosen for our application.

A 0.8-μm SOG layer is coated on the bonded chip and holder by spinning SOG first at 150 rpm for 5 s, and then at 3000 rpm for 20 s. The dispensed volume of SOG for the coating is 1 mL. The slow spin helps SOG to distribute itself uniformly and enter the gap between the chip and the holder, where as the higher spin speed planarizes the top surface [Fig. 2(g)].

The gap-filling behavior of SOG during spin-coating is mainly due to the capillary effect. This capillary effect, and thereby the gap-filling performance, can be enhanced by raising the surface wettability [11]. Hence, before spinning SOG, the bonded chip and holder are treated with oxygen plasma (O_2 flow rate 20 sccm, RF power 100 W, chamber pressure 300 mTorr) for 5 min to improve the surface wettability. After the spin, SOG is soft-baked on a hot plate sequentially at 80, 150, and 250 °C, each for a minute. The same coating and baking process is repeated two more times to ensure a complete gap-filling between the chip and the holder. At the end, the thick passivation layer that results from multiple coating is thinned down to 1 μm by ICP etch (CHF_3 flow rate 20 sccm, ICP power 900 W, RF power 200 W, chamber pressure 0.5 Pa).

Fig. 5. Vertical displacement of an integrated chip relative to holder where the holder surface corresponds to 0-μm height.

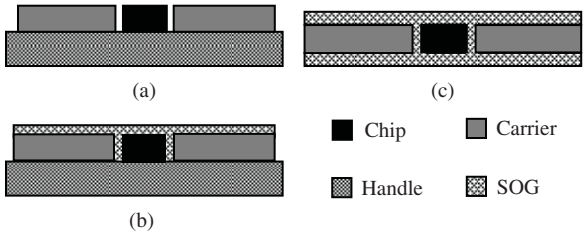


Fig. 6. Process steps to embed a chip using only SOG. (a) The holder and the chip are placed face-down on a handle substrate. (b) SOG is spun on the backside of the chip and the holder to fill the gap and planarize the bottom surface. (c) Handle substrate is removed, and the planarization is performed on the top surface of the chip and the holder.

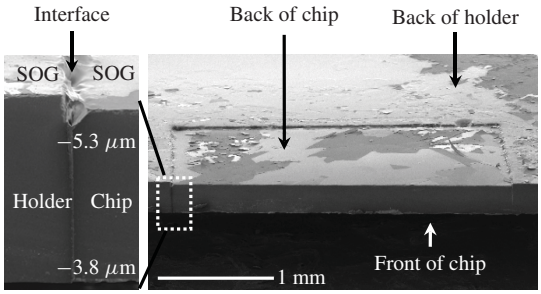


Fig. 7. SEM image of the backside of a chip that was integrated using only SOG.

The SEM cross-sectional image of a packaged chip is given in Fig. 4. As seen from the figure, the gap between the chip and the holder is completely filled with SOG. The variation in gap size between top and bottom is due to the undercut profile resulting from the DRIE Bosch process. The difference in height between the chip and the holder is measured by a Dektak profilometer (Fig. 5). The vertical displacement of the chip relative to the holder is approximately 0.5 μm.

D. SOG Packaging

We have also implemented a simplified version of the integration scheme discussed in Sections II-A–C. The method obviates the use of a carrier wafer for the integration. After placing the chip and the holder face-down on a handle wafer, SOG is spin-coated three times on the backside of the chip and the holder [Fig. 6(a) and (b)]. This results in complete gap-filling from the backside, and planarization of the bottom surface. The baking of SOG is performed on a hot plate sequentially at 80, 150, and 250 °C, each for a minute after each spin. The top surfaces of the chip and the holder are then planarized with SOG by following the same process as described in Section II-C [Fig. 6(c)].

The SOG film coated on top and bottom is found to be strong enough to hold the chip firmly inside the holder wafer during any subsequent process steps. Fig. 7 shows the SEM image of the backside of a chip that is integrated by applying the abridged packaging method. As seen from the figure, SOG planarizes the bottom surface of chip and holder with complete gap filling.

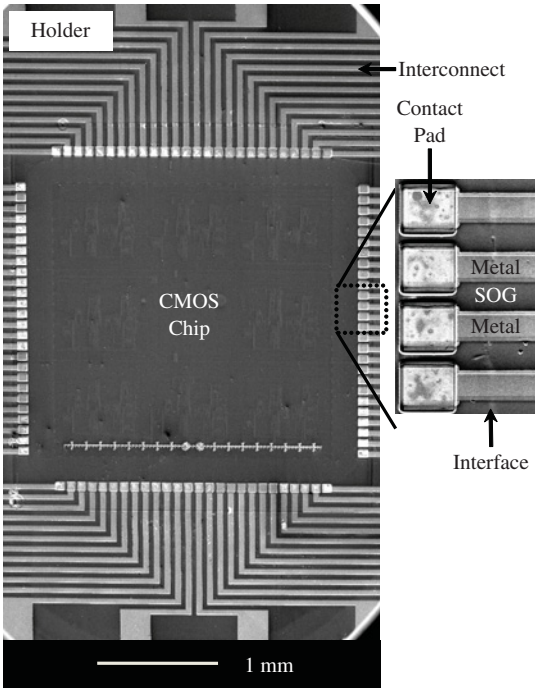


Fig. 8. SEM micrograph of patterned interconnects.

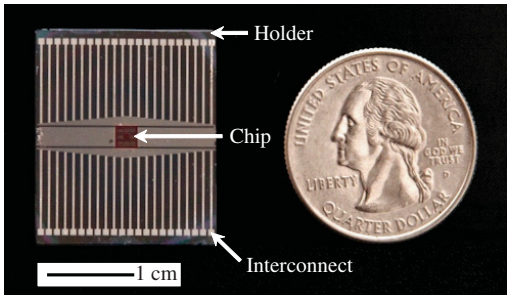


Fig. 9. Image of a chip that was successfully integrated and post-processed.

E. Contact Pattern

In this part of the process, vias to the perimeter pads of the chip are created, and interconnect lines are patterned that extend from the chip to the holder.

Initially, contact vias are patterned by spinning resist and photolithographically opening the contact pads. Access to the

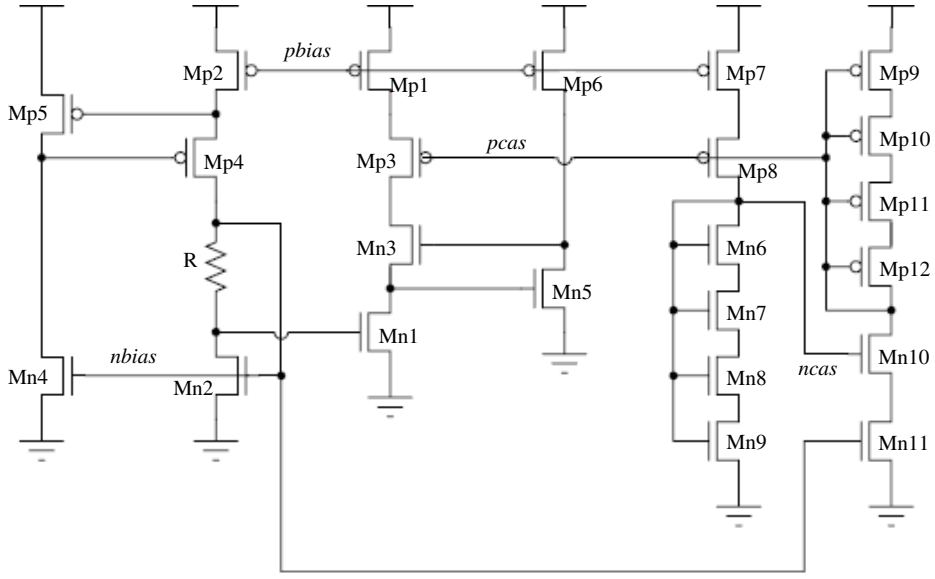


Fig. 10. Supply independent current source circuit of the CMOS chip.

TABLE I
TEST RESULTS OF BARE AND INTEGRATED DIES AT $V_{dd} = 5$V

	pbias	*pcas*	*Ncas*	*nbias*
Unpackaged chip (V)	3.648	3.197	1.844	1.383
MOSIS packaged chip (V)	3.648	3.215	1.826	1.376
Integrated die meas. 1 (V)	3.547	3.124	1.846	1.374
Integrated die meas. 2 (V)	3.542	3.129	1.841	1.378
Integrated die meas. 3 (V)	3.544	3.128	1.842	1.371
Integrated die meas. avg. (V)	3.544	3.127	1.843	1.374
Supply current (mA)	10.00	10.00	10.00	10.00
Trace resistance (Ω)	8.00	8.00	8.00	8.00
Supply IR drop (V)	0.08	0.08	0.08	0.08
Effective bias (V)	3.624	3.207	1.843	1.374
Difference voltage (V) (bare die versus integrated die)	0.024	−0.010	0.001	0.009

TABLE II
TEST RESULTS OF INTEGRATED DIES AT DIFFERENT V_{dd}

V_{dd} (V)	*pbias* (V)	*pcas* (V)	*ncas* (V)	*nbias* (V)
5	3.544	3.127	1.843	1.374
4	2.552	2.137	1.777	1.315
3	1.558	1.165	1.758	1.3

aluminum pads are made by etching via holes in SOG using the resist as a mask [Fig. 2(h)]. SOG is etched using CF_4/O_2 (CF_4/O_2 flow rate 50 sccm/10 sccm, ICP power 200 W, RF power 50 W, chamber pressure 0.5 Pa).

After opening the contact vias, metal interconnects are patterned by applying lift-off of metal [Fig. 2(i)]. First, the lift-off pattern is made by lithography using the negative resist, nLOF2070. A 500 nm aluminum layer is deposited on the top surface by electron beam evaporation. Metal lift-off is then performed in Shipley Microposit Remover 1165 at 80 °C.

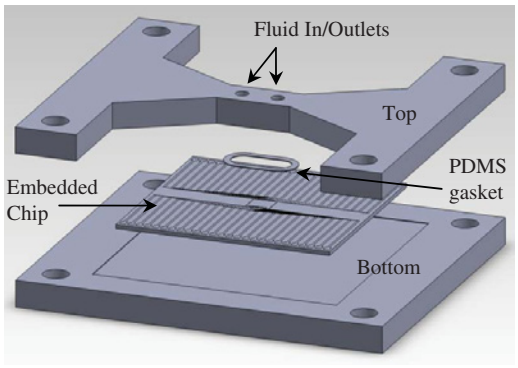
Fig. 8 shows the SEM image of interconnects on the packaged chip. A total of 104 interconnects are patterned from the chip to the holder. The interconnect line resistance is measured to be 4 Ω approximately. The contact pads of the chip are 78 μm × 78 μm, with a center-to-center pad distance of 90 μm. A photograph of the packaged chip is given in Fig. 9.

III. ELECTRICAL CHARACTERIZATION OF CIRCUIT

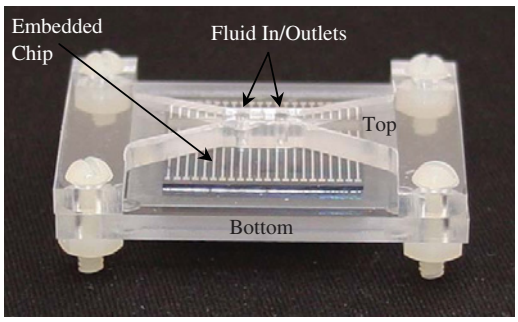
The effect of the integration process on the circuit performance has been evaluated. A key circuit in most analog processing blocks is a supply independent current source which serves as the ideal test circuit. One of the main reasons why this block serves as an ideal process indicator is that the bias voltages are directly proportional to process parameters, which are reflected in the unified parameter of threshold voltage. Threshold variations can cause functional failures, slower operating speeds or reduced dynamic range. A schematic of the supply independent current source is given in Fig. 10. The value of *nbias* can be calculated by equating the currents in transistors Mn1 and Mn2, and is given as follows:

$$nbias = V_{gsMn1} = \frac{2}{R\left(\frac{\mu_n C_{ox}}{2}\frac{W_{Mn2}}{L_{Mn2}}\right)} + V_{tn} \qquad (1)$$

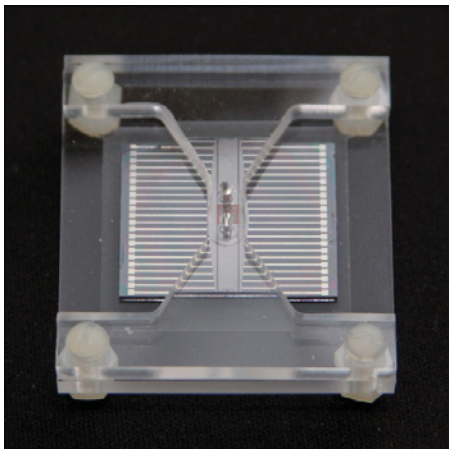
where μ_n is the electron mobility, C_{ox} is the gate oxide capacitance, V_{gs} is the gate-source voltage, V_{tn} is the threshold voltage of nMOSFET, L and W are the length and the width of the device channel and R is the resistance. The circuit forces a V_{tn} referenced *nbias* voltage by the action of a self-biased negative feedback loop. The *pbias* voltage is due to the action of a diode connected PMOS device and hence is V_{tp} referenced. Thus by measuring these voltages we can infer the effect of the process on the CMOS device parameters. In addition to measuring the *nbias* and *pbias*



(a)



(b)



(c)

Fig. 11. (a) Assembly of a CMOS/microfluidic hybrid system. The VCSIT encapsulated chip is sandwiched between two acrylic parts where the fluidic channel lies in the top acrylic part. A PDMS gasket provides watertight seal between chip and fluidic channel. (b) Side-view. (c) Top-view of the final CMOS/microfluidic hybrid system.

voltages, we also measured the cascode transistor (common-gate gain boosting) bias voltages, *ncas*, and *pcas* to further validate the measurements.

Table I presents the parameter values of the circuit measured on a bare die and an integrated die. For comparison purposes, values from a packaged chip by MOSIS are also included. As seen from the table, the measurements of the packaged and unpackaged chips match very well. After the integration the values of *pbias* and *pcas* have larger differences than the *nbias* and *ncas* measurements. However, since there is only one V_{dd} and *Gnd* pad on this particular chip, and given that 10 mA current is drawn from the supply by the chip, a total interconnect trace resistance between V_{dd} and *Gnd* of 8 Ω yields a total *IR* drop of 80 mV. This supply drop only affects *pbias* and *pcas* and not *nbias* and *ncas*. This was verified by measuring the bias voltages for various V_{dd} supplies, as given in Table II. Making the appropriate corrections yields a very modest difference between the bare and integrated dies, demonstrating that the process does not affect the circuit parameters.

IV. Discussion

VCSIT offers a number of important advantages over other SIP technologies reported before. For example, multichip module and SAWLIT used top passivation layers of thickness, 25 and 6 μm, respectively, [1], [6]. Vias to metal pads are then created by patterning the passivation layers. A thick passivation layer, and as a result deep vias, necessitates the deposition of a thick metal layer to ensure complete step coverage for making metal interconnects from chip to substrate. On the other hand, the micrometer thick passivation layer achieved with VCSIT results in a small step height from the metal pads to the top surface of the chip. In our case, the step height was 2.8 μm including the thickness of the passivation layer. Although thicker metals can be deposited for higher current applications, it is found that the deposition of even a relatively thin metal layer (200 nm) is sufficient to cover this via step completely. More importantly, the resulting thin passivation layer is less prone to introducing misalignment during the contact lithography due to the tight gap between the mask plate and the chip surface. Thus, VCSIT has considerably higher alignment accuracy in subsequent lithographic steps.

In VCSIT, chips are positioned in a self-aligned manner as a result of the tight gap that exists between the chip and the wafer. Thus the margin of misalignment is very small (few micrometers) during the placement of the chip. The SAWLIT process can only integrate chips which are of the same size. In this process, the chip housing in the holder wafer was about 10 μm larger on each side of the chip. Substantial optimization of the DRIE process was required to achieve the 10-μm gap. On the other hand, the chip-based lithography technique of VCSIT is not only able to accommodate for the variation in chip size, but also to create the gap size as small as 4 μm without any optimization of the DRIE process. It is possible to make the gap even smaller

with further optimization, thereby increasing the precision in chip alignment. High-accuracy alignment is critical for the integration of multiple dies in a large holder, especially to achieve ultrahigh lead-count interconnects.

Earlier SIP technologies used PDMS, SU8, Polyimide, Parylene C, etc., for planarization or gap-filling [1]–[6]. All these polymers possess many attractive features: biocompatibility, low dielectric constant, flexibility, ease of processing, etc. However, some drawbacks are associated with these polymers which make them incompatible with either biological, CMOS or MEMS platform. PDMS has a low thermal conductivity and to maintain its chemical and physical properties, the temperature cannot exceed 200 °C. Hence PDMS should not be used for applications where heat dissipation is critical, or operating temperature goes above 200 °C [6]. In addition, PDMS is not compatible with non-polar and less-polar solvents such as acetone, chloroform, ether, etc., since these solvents diffuse into PDMS and cause it to swell [15]. SU-8 suffers from crack formation during the post-exposure bake due to the cross-linking of SU-8. Due to the mismatch of the coefficient of thermal expansion between SU-8 and substrate, internal stress is induced in the resist and bowing of substrate has been observed [16]. Polyimide has relatively high moisture uptake (4–6%). Some polyimides have lower moisture absorption, but they require high-temperature curing steps [3]. Parylene C has poor adhesion to underlying materials although an improvement in adhesion with a few materials has been demonstrated using an adhesion promoter [17]. SOG and BCB were chosen for planarization and bonding in VCSIT. SOG and BCB are widely used in the integrated circuit (IC) and MEMS industry as interlayer dielectric [11], [18], passivation [22], [23], planarization [19], [20], and bonding materials [8], [21], because of their low dielectric constant, low-temperature process conditions and excellent chemical resistance. BCB is one of the preferred materials for biological applications since it has a very low moisture uptake (<0.2%) [10]. The excellent properties of BCB and SOG make VCSIT bio-, MEMS, and post-CMOS compatible. However, random cracks were observed in the SOG film across the gap between the chip and the holder. This could be due to the thermal stress induced in thick SOG sandwiched between the chip and the holder [24]. The cracks were 100–300 nm wide. The cracks were filled by the plasma-enhanced chemical vapor deposition of a 200-nm oxide layer.

The cost-effectiveness of VCSIT needs to be emphasized. Conventionally, space is allocated on the CMOS chip for the fabrication of large passive components and MEMS structures [25], [26]. Utilizing VCSIT, large passives and MEMS structures can be integrated with the packaged chip as disparate components by post-integration micromachining instead of on-chip fabrication. This can be achieved following a fabrication process similar to the one demonstrated by Rodger *et al.* with their CL-I^2 technology where off-chip RF-MEMS inductor coil is post-fabricated with the Parylene C encapsulated chip on the same platform [4]. Interconnects from the chip to the off-chip passives can then be patterned by standard photolithography. This will provide more integration flexibility, and decrease the complexity and cost of IC fabrication. Furthermore, the technology will facilitate the visual inspection of interconnects which is not possible in techniques such as flip-chip bonding [27].

VCSIT facilitates the seamless integration of microfluidic channels on top of the CMOS chip. The major bottleneck in microfluidic-CMOS integration is that the footprint of microfluidic systems generally exceeds the size of the CMOS chips. In order to facilitate the fabrication of microfluidic systems, the chip area needs to be increased to match the size of microfluidic systems. VCSIT offers a cost-effective way to increase the footprint by embedding the chip in a large substrate that serves as a platform for the subsequent fluidic integration. Fig. 11(b) and (c) shows a CMOS/microfluidic hybrid system based on the VCSIT. The embedded chip is inlaid on an acrylic stage, and mechanically secured by fastening an acrylic microfluidic channel on top [Fig. 11(a)]. A PDMS gasket is used to achieve a tight seal between chip and fluidic channel. After the integration of the fluidic channel, the pads of the CMOS chip can be accessed for electronic measurements via interconnect pads at the edge of the carrier. Various biosensing experiments are currently underway utilizing the proposed VCSIT microfluidics.

VCSIT process can be easily extended to integrate multiple dies on the same wafer. The central issues with the multi-chip alignment are die-edge roughness due to the thickness of the dicing saw, and die placement accuracy. Die-edge roughness can be addressed following a process developed in [28] which involves DRIE and ultraprecision grinding after initial dicing of chips. This process can achieve die-edge precision of 0.5 μm. Such precision will allow us to use a fixed-size photomask for patterning cavities for multiple dies on the same wafer. The placement of each die can be achieved with a precision of 0.5 μm using a state-of-the-art bonder such as the *fineplacer lambda die bonder* from finetech GmbH. Using these methods, die-to-die alignment accuracy within 2 μm and die-to-reference structure alignment within 1 μm could be achieved. The free space between each die and holder needs to be greater than the combination of the die-edge precision, die-placement tolerance and lithographic tolerance for patterning the cavities.

V. Conclusion

A novel self-aligned chip-specific wafer level integration technology concept was presented. Due to the chip-based lithography approach, the technique allows the creation of a very tight fit between the chip and the holder. The small vertical displacement between the chip and the holder, and the thin passivation layer on top allow for high-accuracy alignment during any post-integration fabrication processes. Thus, VCSIT has the potential to accomplish high-precision multichip integration with high-resolution, and ultraHDIs. In addition, the VCSIT platform has been designed with CMOS-, MEMS-, and bio-compatible materials and processes. It allows for microfluidic integration and post-CMOS micromachining of the packaged chip. To validate the VCSIT, a low-power potentiostat CMOS chip was integrated using silicon substrates. HDIs were patterned on top of the packaged chip.

Electrical measurements on the supply current source of the chip show that the post-integration processing does not affect the CMOS device parameters.

Because of its versatility, the VCSIT promises to be a formidable approach to implement next-generation biochips, integrated CMOS RF ICs and photonic CMOS chips.

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