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Integration of solid-state nanopores in a 0.5 μm CMOS foundry process

A Uddin, S Yemenicioglu, C-H Chen, E Corigliano, K Milaninia and L Theogarajan

Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106, USA

E-mail: ltheogar@ece.ucsb.edu

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Abstract

High-bandwidth and low-noise nanopore sensor and detection electronics are crucial in achieving single-DNA-base resolution. A potential way to accomplish this goal is to integrate solid-state nanopores within a CMOS platform, in close proximity to the biasing electrodes and custom-designed amplifier electronics. Here we report the integration of solid-state nanopore devices in a commercial complementary metal–oxide–semiconductor (CMOS) potentiostat chip implemented in On-Semiconductor's 0.5 μm technology. Nanopore membranes incorporating electrodes are fabricated by post-CMOS micromachining utilizing the n+ polysilicon/SiO_2/n+ polysilicon capacitor structure available in the aforementioned process. Nanopores are created in the CMOS process by drilling in a transmission electron microscope and shrinking by atomic layer deposition. We also describe a batch fabrication method to process a large of number of electrode-embedded nanopores with sub-10 nm diameter across CMOS-compatible wafers by electron beam lithography and atomic layer deposition. The CMOS-compatibility of our fabrication process is verified by testing the electrical functionality of on-chip circuitry. We observe high current leakage with the CMOS nanopore devices due to the ionic diffusion through the SiO_2 membrane. To prevent this leakage, we coat the membrane with Al_2O_3, which acts as an efficient diffusion barrier against alkali ions. The resulting nanopore devices also exhibit higher robustness and lower $1/f$ noise as compared to SiO_2 and SiN_x. Furthermore, we propose a theoretical model for our low-capacitance CMOS nanopore devices, showing good agreement with the experimental value. In addition, experiments and theoretical models of translocation studies are presented using 48.5 kbp λ-DNA in order to prove the functionality of on-chip pores coated with Al_2O_3.

S Online supplementary data available from stacks.iop.org/Nano/24/155501/mmedia

(Some figures may appear in colour only in the online journal)

1. Introduction

Genes, proteins and other biomolecules provide a wealth of information that is essential for the diagnosis and treatment of diseases. One of the key bottlenecks to the widespread use of personalized medicine is the lack of a low-cost, high-throughput, accurate and easy-to-use biomolecule detection platform. The realization of such a detection platform will also aid in the early detection of disease, which in cases such as cancer greatly enhances the survival rate. Fundamentally, sensing results in a binary response to the presence or absence of a particular target. Nature accomplishes this complex task, with exquisite precision, by utilizing channels or pores combined with molecular recognition. The mechanism often involves the gating of ion fluxes though nanometer sized molecular pores or channels. This change in ion flux then regulates other pathways either directly or via secondary pathways.

Recently, inspired by biology, nanopores have emerged as a possible single-molecule electronic detection plat-

form [1–3]. A nanopore is an extremely tiny hole, a few nanometers in diameter, in an insulating membrane that separates two ionic reservoirs. An applied voltage across the nanopore results in an ionic current that flows through the nanopore. The principle of single-molecule detection using the nanopore is based on detecting the blockage of this ionic current by the target. The first application of nanopores to biosensing was performed using a biological pore, α-hemolysin, for the possible sequencing of DNA. Initially, it was hoped that molecular size and nature of functional groups of each nucleobase would result in an appreciable change in ionic current as the DNA threaded through the nanopore [4]. Unfortunately, though some ionic current changes were observed, they were not due to the single nucleobase differences but rather due to folding and stacking effects [5]. Since then there has been intense activity, in both academia and industry, towards realizing a single-molecule detector based on the nanopore, and many excellent reviews are available [1–3]. Recent advances include solid-state nanopores [1], biological pores modified with molecular adaptors [6] and single-base detectors that couple exonuclease activity and the nanopore [7].

One of the primary reasons for such a vigorous effort in the field of nanopore sensors is their promise of realizing fast, cheap, reliable and label-free sensors, especially for DNA sequencing. Compared to existing methods of DNA sequencing that require several thousand dollars and many weeks to complete a sequence [8], nanopores have the potential to reduce the time to a few days at a significantly lower cost, though many challenges are to be overcome. One of the primary challenges that have been identified is the integration of the nanopore platform and potentiostat electronics [1]. A potentiostat enables the application of a fixed potential across the membrane and measures the current going through the nanopore. An efficient integrated platform will reduce the parasitic capacitance and enable a wider bandwidth and a lower-noise operation, which can greatly enhance the sensitivity of the nanopore. Recently, it has been demonstrated that by simply placing an integrated potentiostat chip close to a separate nanopore chip vastly larger bandwidths could be achieved [9]. We believe this can be further enhanced by coupling the circuit and the nanopore more intimately. Additionally, by coupling the nanoscale sensor and the sensing electronics, closed-loop feedback can be implemented that can increase the dynamic range of the sensor. Furthermore, due to the batch fabrication nature of IC processes, massively parallel sensors with integrated electronics can be built. This is a crucial step if on-chip sequencing or massively parallel biosensing is to become a reality.

This paper reports on the fabrication and characterization of integrated solid-state nanopore devices in a standard complementary metal–oxide–semiconductor (CMOS) potentiostat chip. Each step in the fabrication process was carefully optimized to ensure compatibility with the CMOS process. This is validated by the electrical characterization of the on-chip CMOS circuitry after every process step. In addition, the low complexity of the proposed process results in high device yield. The bulk properties of the membrane were studied by transmission electron microscopy (TEM), energy dispersive x-ray spectroscopy (EDX), and electron energy loss spectroscopy (EELS). We also present a method to batch process a large of number of identical nanopore devices across large CMOS-compatible wafers by electron beam lithography (EBL). The integrity of both CMOS and CMOS-compatible nanopore devices is demonstrated by measuring the conductance, capacitance and noise characteristics. The functionality of these nanopores in the CMOS chip was also demonstrated through the detection of 48.5 kbp double-stranded λ-DNA in 1 M KCl under an applied electric field.

2. Fabrication and characterization

2.1. Fabrication of oxide membrane in CMOS

Our custom-designed CMOS potentiostat chip is 1.7 mm $\times$ 1.7 mm $\times$ 260 μm, implemented in On-Semiconductor's C5N 0.5 μm technology (figure 1(a)). This technology is a low-cost, non-silicided CMOS process facilitating stacked contacts with three metal layers and two highly n-doped polysilicon layers. Figure 2(a) shows a schematic cross-section of the CMOS circuitry in On-Semiconductor's 0.5 μm process. To make highly sensitive nanopore devices, we have utilized the polysilicon–insulator–polysilicon (PIP) structure available in this process [10]. Doped polysilicon layers, having thicknesses of 370 nm and 250 nm in this capacitor, are used as biasing electrodes across the nanopore. The insulator sandwiched between the polysilicon layers is a thin (35 nm) silicon dioxide layer where the synthetic membrane containing the pore is fabricated. The PIP capacitor is chosen over other types of capacitor, such as the metal–insulator–metal (MIM) capacitor, because insulators in PIP capacitors are deposited by sophisticated chemical vapor deposition (CVD) techniques such as low-pressure chemical vapor deposition (LPCVD), and they are of higher quality [11]. On the other hand, insulators in MIM capacitors are usually deposited by plasma enhanced chemical vapor deposition (PECVD). PECVD insulators are more prone to defects or pinholes. As a result, they are lower-quality insulators. In addition, polysilicon layers in PIP are more mechanically robust and show better chemical resistance as compared to the metal layers of MIM [11]. The inset of figure 1(a) shows an expanded image of the PIP capacitor. The size of the bottom polysilicon (Poly 1) and top polysilicon (Poly 2) layers are 150 μm $\times$ 150 μm and 15 μm $\times$ 15 μm, respectively. An SEM cross-section of the PIP capacitor along the AB direction (as indicated in the inset of figure 1(a)) is given in figure 1(b). The inset of figure 1(b) clearly shows different layers of PIP capacitor with the underlying field oxide (FOX) and silicon substrate.

Nanopore devices with adjacent electrodes were fabricated in the CMOS chip by applying post-CMOS micromachining (figure 2(b)). First the custom-designed CMOS potentiostat chips were fabricated via the metal–oxide–semiconductor implementation service (MOSIS). The process flow to fabricate oxide membranes in CMOS chips is given in

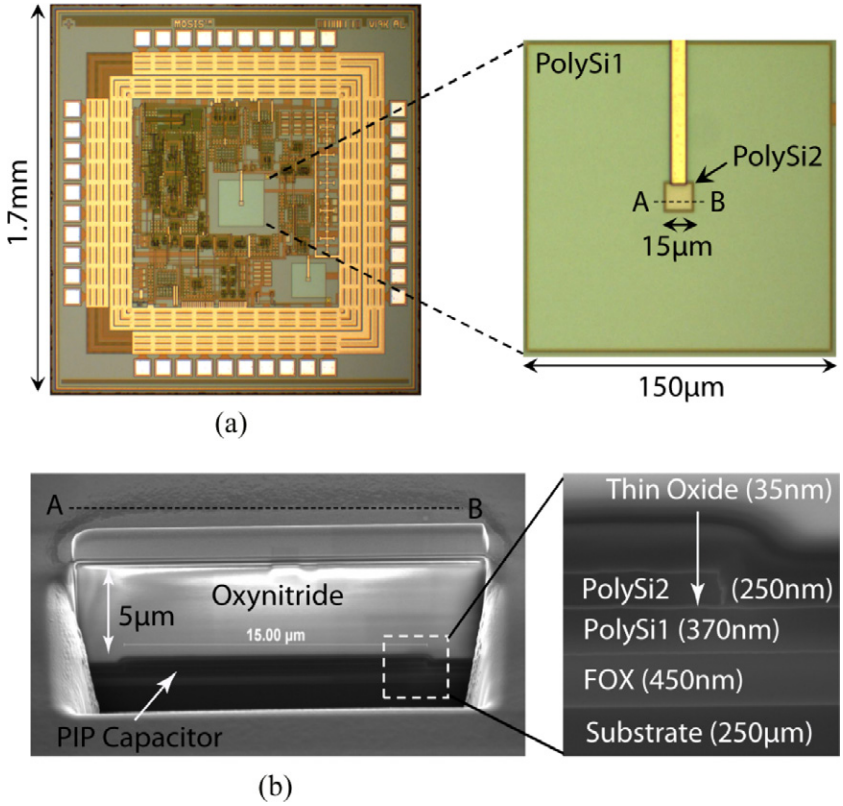

Figure 1. (a) Optical micrograph of the CMOS potentiostat chip implemented in On-Semiconductor's 0.5 μm technology. The inset shows an expanded image of the PIP capacitor that is utilized to fabricate nanopore devices and electrodes. (b) SEM cross-section of the PIP capacitor along the AB direction as indicated in the inset of (a). The inset shows a magnified view of the capacitor, FOX and substrate.

figure 2(c). For simplicity, only the PIP capacitor portion of the chip is included in this flow. The process starts with the deposition of a 500 nm thick Si_3N_4 passivation by PECVD on the backside of the CMOS chip (figure 2(c)(i)). A 5 μm square window was then lithographically patterned on the frontside of the chip. The pattern was transferred to the oxynitride passivation (thickness ~5 μm) by inductively coupled plasma etch (ICP) (CHF_3 flow rate 20 sccm, ICP power 900 W, RF power 200 W, chamber pressure 0.5 Pa) (figure 2(c)(ii)). The chip was then flipped and a 100 μm square window was patterned on the backside. Nitride passivation at the bottom was removed by ICP etch using the aforementioned process conditions. This was followed by the anisotropic etching of silicon substrate by deep reactive ion etch (DRIE) using FOX as etch-stop (figure 2(c)(iii)). After this, the FOX layer was etched in ICP (figure 2(c)(iv)). A 100 nm Al_2O_3 film was then deposited by atomic layer deposition (ALD) on the backside of the chip to isolate the bulk silicon substrate from the ionic solution and prevent a short electrical path during the subsequent electrochemical characterization of nanopore devices (figure 2(c)(v)). A short ICP etch anisotropically removed Al_2O_3 that was deposited underneath the Poly 1 layer (figure 2(c)(vi)). In the final step, a free-standing oxide membrane was created by etching the polysilicon layers in XeF_2 (figure 2(c)(vii)). Figures 3(a) and (b) show SEM micrographs of the top and cross-section of a fabricated SiO_2 membrane in the CMOS chip. The thickness of the membrane obtained from SEM was 35 nm. This thickness was also confirmed by measuring the electron energy loss spectrum (EELS) of the membrane by employing an FEI Titan FEG TEM with a Gatan Enfina EELS spectrometer at an accelerating voltage of 300 kV (figure 3(c)). The thickness of the membrane is obtained from the log-ratio method [12] using the following expression:

$$t = \lambda \ln \frac{I}{I_0} \tag{1}$$

where λ is the mean free path of inelastic electron scattering in oxide, I is the integrated intensity under the total EEL spectrum and I_0 is the integrated intensity under the zero loss peak (ZLP). The thickness calculated from this method is 37.8 nm, which is close to the value from SEM. In addition, energy dispersive x-ray spectroscopy (EDX) was performed to determine the elemental composition of the membrane. Figure 3(d) shows the EDX spectrum recorded from the oxide membrane in the CMOS chip. Strong peaks were observed in the EDX spectrum at x-ray energies that are characteristic of silicon and oxygen. Compositional analysis revealed 31% Si and 69% O, which is in good agreement with the expected stoichiometric film ratio of 33.33% Si and 66.67% O.

2.2. Post-fabrication characterization of CMOS

The post-CMOS micromachining process of a CMOS chip needs to be carefully planned and implemented so that the process is non-destructive to on-chip circuitry. There are

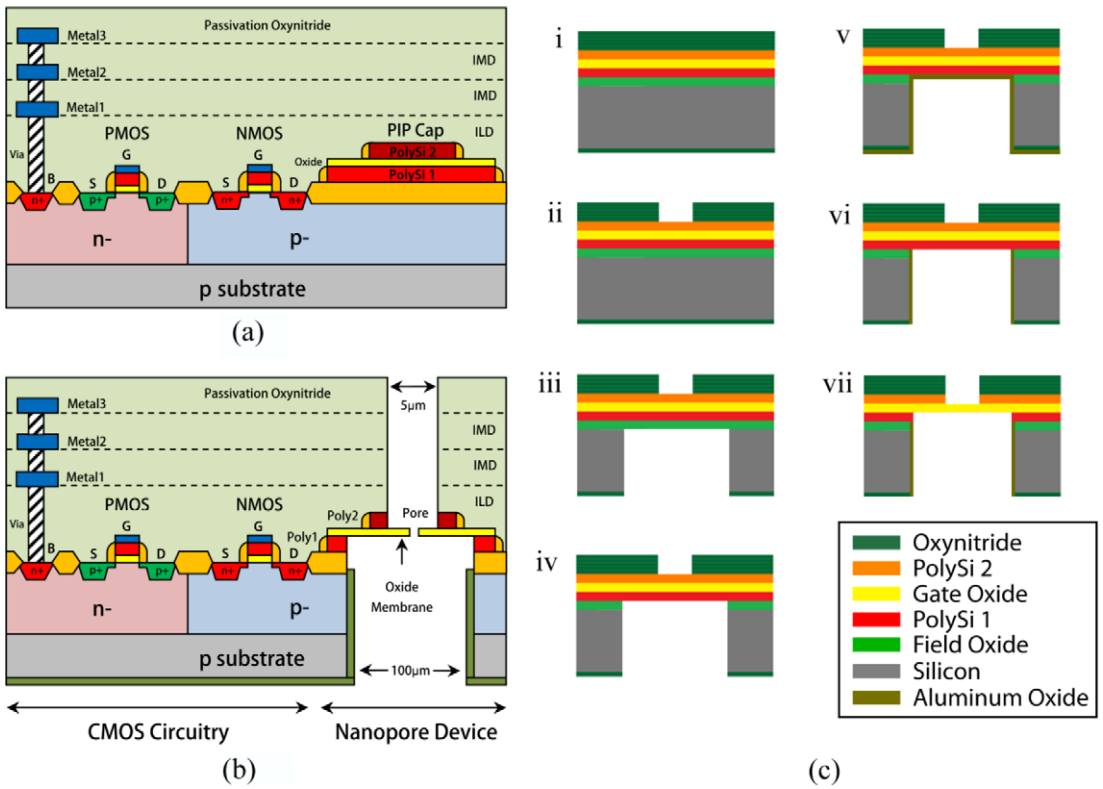

Figure 2. (a) Cross-sectional schematic of a CMOS integrated chip implemented in On-Semiconductor's 0.5 μm process. (b) Cross-sectional representation of the same technology after the fabrication of nanopore devices and electrodes utilizing a PIP capacitor in close proximity to the CMOS amplifier circuitry. (c) Process flow to create oxide membranes and electrodes in the PIP capacitor. (i) Passivation of the backside of the chip with PECVD Si_3N_4. (ii) Patterning of a 5 μm $\times$ 5 μm window on the frontside and etching the oxynitride passivation. (iii) Opening a 100 μm $\times$ 100 μm window on the backside. Etching of the nitride passivation by ICP and the silicon substrate by DRIE. (iv) Removal of FOX by ICP etch. (v) Deposition of Al_2O_3 by ALD on the backside for isolation of the bulk substrate. (vi) Etching of Al_2O_3 under the Poly 1 layer by ICP. (vii) Creation of membranes and electrodes by removing polysilicon layers by XeF_2 etch.

various factors that need to be considered in post-CMOS micromachining. (1) Process steps must be compatible with the existing materials in the chip. (2) Adhesion of any deposited material on the exposed surface of the chip needs to be carefully evaluated with due consideration of process compatibility. (3) Post-CMOS micromachining imposes a strict thermal budget (<450 °C), due to the degradation of on-chip metal layers above this temperature [13]. Additionally, high temperature can result in cracks due to the mismatch of thermal expansion coefficients of films. (4) Plasma processes used for the deposition and etching of materials can cause breakdown or degradation of gate dielectric in transistors due to the plasma induced charge accumulation in the dielectric [14]. (5) Owing to the small size, the chip needs to be handled carefully to prevent breakage and contamination. Due to the large number of constraints imposed, it is important to verify that the performance of CMOS circuitry is unchanged after each fabrication step.

To verify that our process is CMOS-compatible, electrical measurements were performed on a *supply independent current source circuit* already present on the CMOS potentiostat chip. The reason this circuit serves as an ideal process indicator is that the bias voltages are directly proportional to process parameters, which is reflected in the unified parameter of threshold voltage [15]. Threshold variations can cause functional failures, slower operating speeds or reduced dynamic range. A schematic diagram of the supply independent current source is given in figure 4.

Table 1 lists the voltage values at critical nodes of the circuit, labeled as pbias, pcas, ncas and nbias, measured on an unprocessed die and a processed die after every fabrication step. The measured voltages on the unprocessed and processed chips match very well. This proves that our fabrication process does not have any detrimental effect on the CMOS circuitry.

2.3. Reliability of CMOS membrane

To investigate the reliability of fabricated membranes in CMOS chip, we measured ionic conductance through membranes containing no pores. Figure 5(a) shows the experimental setup used for this experiment (methods). The CMOS chip was mounted between *cis* and *trans* reservoirs filled with solution, 1 M KCl, 10 mM Tris-HCl buffer, 1 mM EDTA, at pH 8. Using Ag/AgCl electrodes and a potentiostat, a voltage was applied across the membrane and the resulting ionic current was measured.

The current–voltage (I–V) characteristics of the blank CMOS membrane were obtained by sweeping the applied

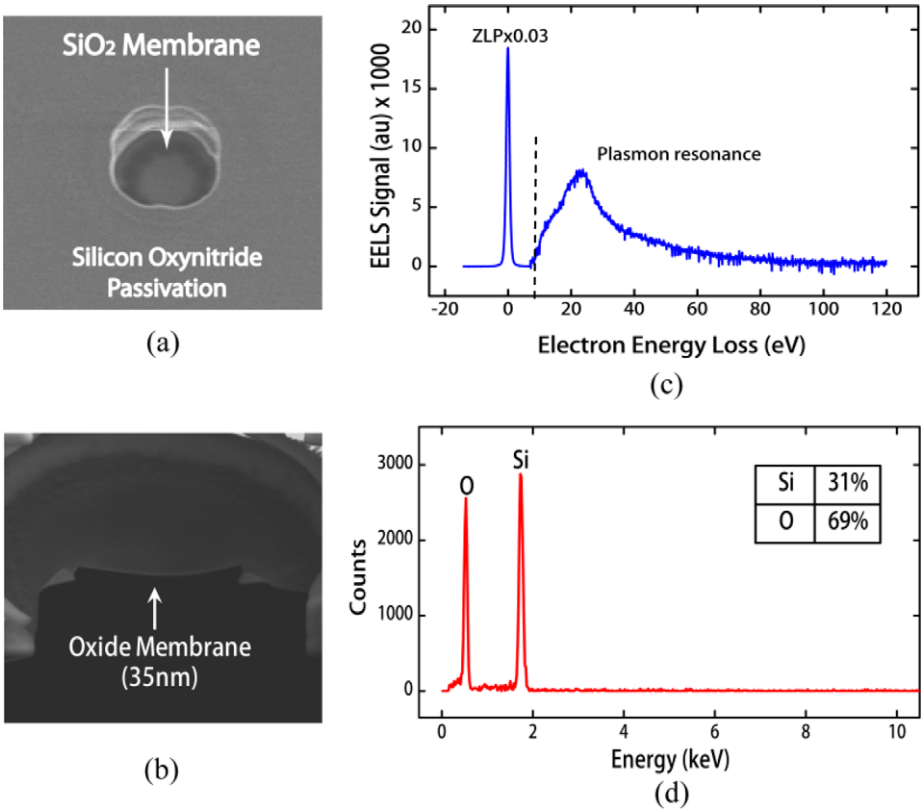

Figure 3. (a) SEM top view of a free-standing SiO_2 membrane fabricated in a CMOS chip. (b) SEM cross-section of the same membrane with thickness ∼35 nm. (c) EELS results of the membrane, which were used to calculate the membrane thickness by applying the log-ratio method. The ZLP in the spectrum is scaled by a factor of 0.03, relative to the rest of the spectrum. (d) EDX spectrum of the membrane illustrating the presence of Si and O, and their composition.

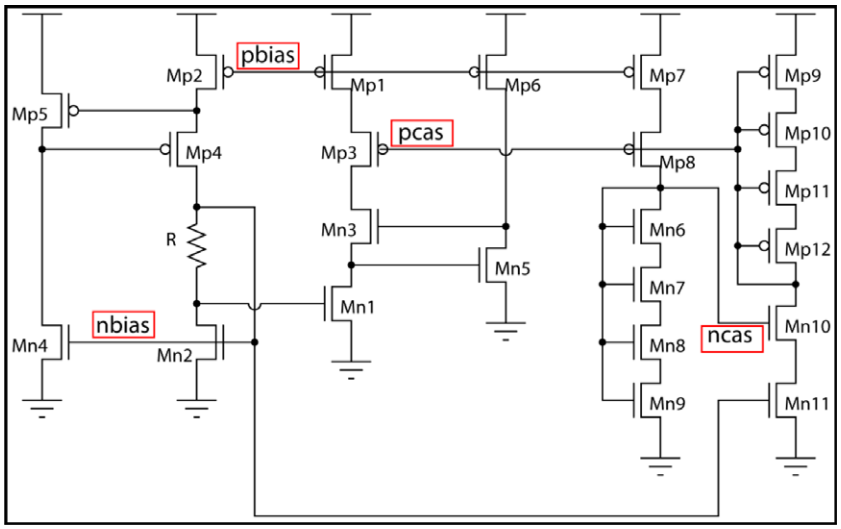

Figure 4. Supply independent current source circuit of the CMOS chip. The circuit was utilized to test the functionality of the CMOS circuitry after every post-CMOS micromachining step.

potential from −100 to 100 mV (figure 5(b), black curve). The current measured with the blank membrane is exceedingly large at all voltages. This large current is a result of the ionic current leakage through the membrane. Since SiO_2 is a relatively low-density (2.2 g cm^{-3}) material, K^+ ions in the buffer solution can drift through it easily under the influence of an electric field [16]. A similar drift phenomenon of alkali ions through gate oxide was previously reported to cause a shift in threshold voltage and introduce instabilities in the operation of a metal–oxide–semiconductor field effect transistor [17]. To prevent ion diffusion through the membrane, we chose to coat it with a high-density

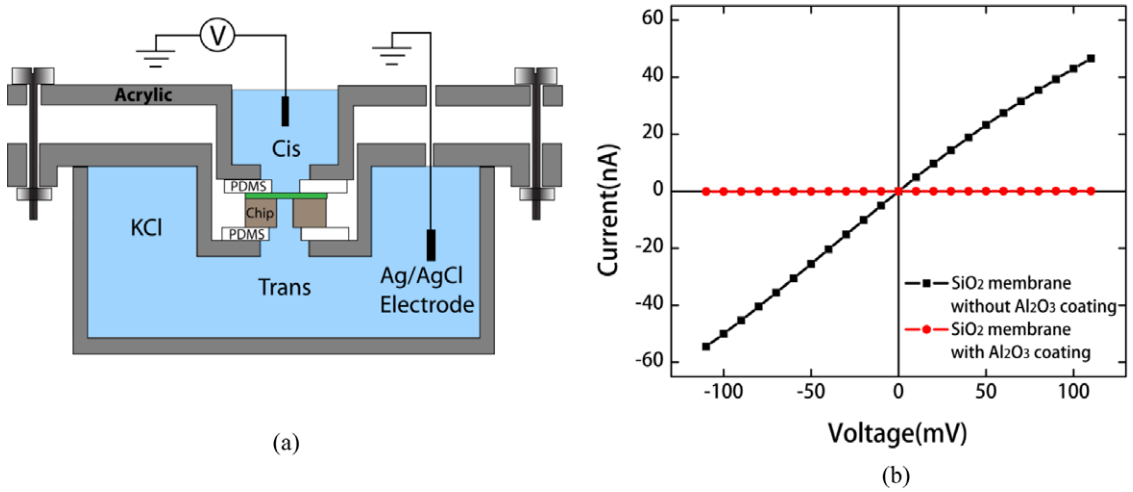

Figure 5. (a) Schematic cross-section of the experimental setup. The CMOS chip containing the membrane was mounted between *cis* and *trans* reservoirs filled with aqueous buffer solution. A patch-clamp current amplifier was used to apply bias across the membrane and measure ionic current. (b) Current–voltage characteristics of a CMOS SiO_2 membrane at 1 M KCl before (black line) and after (red line) the deposition of Al_2O_3 by ALD. Very large conductance was measured with the blank oxide membrane due to the drift of K^+ ions through SiO_2 under applied electric field. Ionic leakage was eliminated by coating the membrane with Al_2O_3.

Table 1. Test results of processed and unprocessed dies at $V_{dd} = 5$ V.

		pbias (V)	pcas (V)	ncas (V)	nbias (V)
Unprocessed chip		3.655	3.200	1.847	1.396
Processed chip	*Fabrication step*				
	After frontside ICP etch of oxynitride	3.637	3.186	1.852	1.406
	After backside Bosch etch of Si	3.633	3.174	1.836	1.378
	After backside ICP etch of FOX	3.639	3.184	1.848	1.399
	After XeF_2 etch of poly-layers	3.645	3.183	1.857	1.403

insulator that acts as a good diffusion barrier against K^+ ions. ALD is the preferred method for uniform coating of dielectrics because it can produce homogeneous films with precise thickness control due to self-limiting growth mechanisms [18]. It is also a low-temperature process (100–300 °C), which makes it compatible with the CMOS process. Other deposition techniques such as LPCVD lack sub-nanometer precision over film thickness, and the elevated deposition temperature (600–800 °C) is not compatible with the CMOS process [19]. Silicon nitride acts as an efficient barrier to mobile ions due to its high density (~3.1 g cm^{-3}) [20], but the deposition of SiN_x by ALD is a challenge because of the preferential reaction of ALD precursors with the oxygen containing species [21]. Hence we opted for a different insulator such as Al_2O_3 that exhibits negligible ion diffusion, and can be deposited by ALD. Al_2O_3 was previously used to develop low-noise and high-throughput nanopore devices [22, 23].

A 30 nm thick layer of Al_2O_3 was deposited by ALD (Methods) on the CMOS membrane, and ionic conductance through the membrane was measured again. Figure 5(b) (red curve) shows the *I–V* characteristics of the Al_2O_3-coated membrane. Clearly, Al_2O_3 coating results in negligible current through the membrane, due to the blockage of mobile ions. Non-zero conductance was measured through the membrane due to the capacitive coupling between measuring electrodes. However, this background conductance is two or three orders of magnitude smaller than the expected conductance of a nanopore. We also explored the long-term reliability of the Al_2O_3-coated CMOS membrane by measuring the conductance through the membrane at regular intervals over an extended period. Conductance values were found to remain stable even after a 12 h period. This validates the chemical and mechanical stability of the Al_2O_3 coated membrane in electrolyte solution.

2.4. Fabrication of CMOS nanopores

Nanopores with relatively large diameter were directly drilled in the SiO_2 membranes of the CMOS chip using a tightly focused electron beam in an FEI Titan field-emission-gun TEM at 300 kV. Al_2O_3 was then deposited by ALD on the membrane to reduce the size of the pores to below 10 nm. The TEM drilling technique in combination with the ALD Al_2O_3 shrinkage allows for robust membranes containing finely tuned pores in the CMOS chip. Figures 6(a) and (b) show the TEM images of a 60 nm SiO_2 pore drilled by TEM, and the corresponding fast Fourier transform (FFT), which confirms the amorphous structure of the pore. The size of this pore was subsequently decreased to 5 nm × 7 nm by ALD Al_2O_3 (figure 6(c)). Bright diffraction spots were clearly

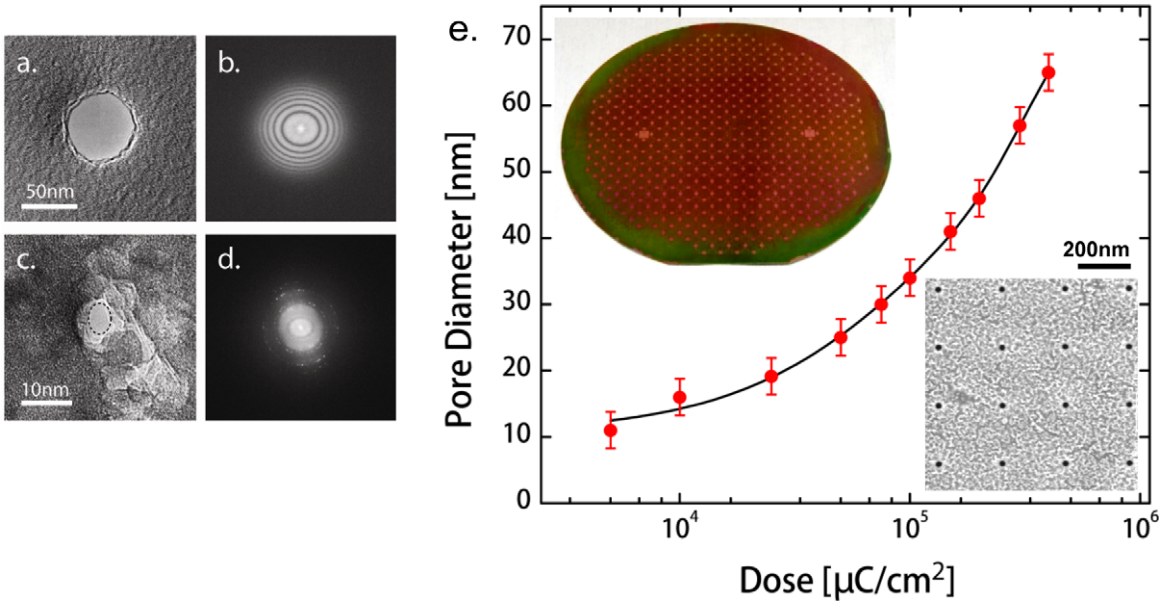

Figure 6. (a) TEM image of a 60 nm CMOS oxide pore that was directly drilled by TEM. (b) Corresponding FFT showing the amorphous structure of the SiO_2 pore. (c) TEM image of the same pore (∼5 nm × 7 nm) after the deposition of Al_2O_3 by ALD. (d) Corresponding FFT indicating the poly-crystalline nature of the Al_2O_3 coated pore. (e) EBL-fabricated pore diameter as a function of e-beam dose on a CMOS-compatible wafer. The top left corner shows a picture of a fully processed 4 in CMOS-compatible wafer containing 19 × 19 membrane chips. An SEM image of an array of ∼25 nm pores fabricated by EBL is given in the bottom right corner.

visible in the corresponding FFT (figure 6(d)), indicating the crystalline nature of the Al_2O_3-coated pore.

2.5. CMOS-compatible wafer-scale nanopores

Wafer-scale processing is an important part of fabricating nanostructures in a cost-effective way. To enable wafer-scale processing, we investigated pore fabrication by electron beam lithography (EBL) as an alternative to TEM drilling. First, we determined process parameters such as etch times for different materials and nanofabrication of pores in separate CMOS-compatible wafers prepared using the same process conditions as the CMOS chip (methods). This enables the tuning of process parameters on relatively inexpensive wafers rather than on fully processed CMOS chips. Nanopores with diameters ∼10–70 nm were then fabricated in the CMOS-compatible membranes across 4 in wafers by EBL with e-beam exposure doses ranging from 5×10^3 to 4×10^5 μC cm^{-2} followed by ICP etch (Methods). Figure 6(e) plots the resulting pore diameter as a function of applied e-beam dose (red symbol). The pore diameter shows a monotonic dependence on the e-beam dose. This trend can be described by the simple equation $d_{\text{pore}} = \alpha D^{\beta}$, with $\alpha \approx 4.76$ nm$(\mu\text{C cm}^{-2})^{-1}$, $\beta \approx 0.43$ and $\chi^2_{\text{red}} = 2.28$ (figure 6(e), black line). The SEM image of an array of EBL-fabricated pores with diameter ∼25 nm is also shown in figure 6(e). A close inspection of 25 nm pores across the wafer revealed variations of ±3 nm in pore diameter. This deviation could be a result of the slight variations in the membrane thickness across the wafer. Unlike the TEM drilling technique, which suffers from low process throughput, the EBL method allows for the production of a large number of identical pores within a single processing batch. However, it is difficult to fabricate sub-10 nm features by the EBL process due to limiting factors such as e-beam scattering [24], resist chemistry [25], and critical dimension loss during pattern transfer [26]. We compensated for this limitation by applying the ALD process and obtained sub-10 nm pores across the CMOS-compatible wafer. Furthermore, the EBL process used to fabricate these pores is CMOS-compatible and readily available in a commercial CMOS foundry, enabling seamless transition to a standard CMOS process. In addition to the EBL approach, we also used these CMOS-compatible wafers to process nanopores by the TEM method to enable measurement of conductance versus pore diameter.

3. Experiments and modeling

3.1. Conductance, noise and capacitance

We measured the ionic conductance of pores in CMOS-compatible chips at high salt concentration. To find the theoretical conductance of the pores, we used geometrical models which assumed a double-conical shape [27, 28] and a hyperboloid [29] shape for the nanopore, incorporating the access resistance outside the pore, as shown in the inset of figure 7(a). These models are characterized by parameters such as total pore length, L, effective pore length, L_{eff}, narrowest diameter of the pore, d, widest diameter of the pore, D, and electrolyte conductivity, σ. The access resistance ($R_{\text{a}} = 1/2\sigma d$) is obtained by considering a planar disc at the pore entrance [30]. As demonstrated previously by Chen *et al* [22], Al_2O_3-coating by ALD reduces the surface charge of nanopores to negligible values. This was further verified

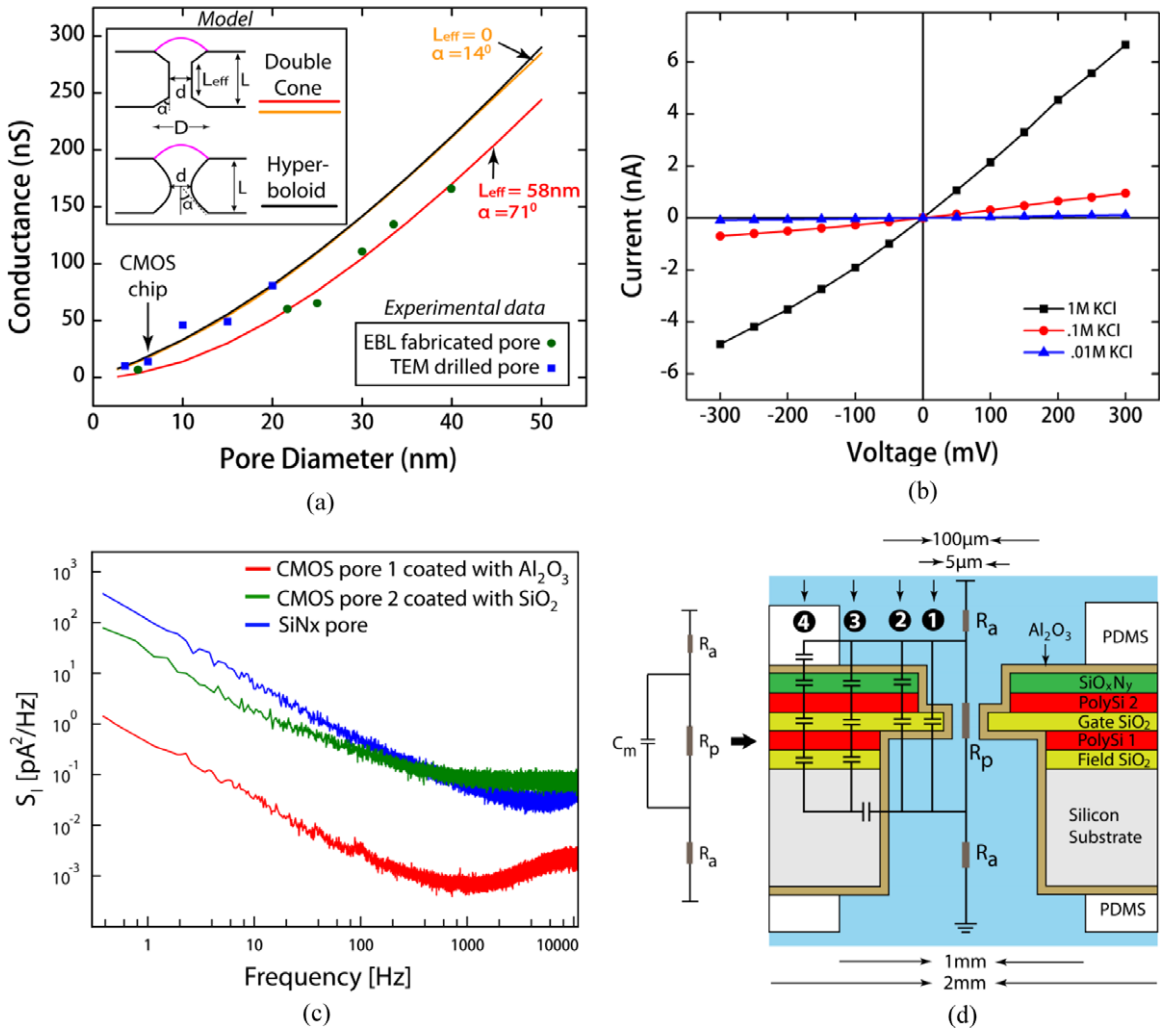

Figure 7. (a) Pore conductance of ten non-CMOS pores and a CMOS pore (indicated by arrow) with diameters 4–40 nm at 1 M KCl. The hyperboloid model with $D = d + 30$ nm (black line) and the truncated double-cone model with $L_{\text{eff}} = 0$ and $\alpha \approx 14°$ (orange line) gave the best fit to the conductance of TEM drilled pores. The EBL fabricated pores were best described by the double-cone conductance model with $L_{\text{eff}} = 58$ nm and $\alpha \approx 71°$ (red line). (b) Current–voltage characteristics of a 5 nm × 7 nm CMOS pore measured in 0.01 M, 0.1 M and 1 M KCl. (c) Power spectral densities of three different nanopores at 100 mV in 1 M KCl. $1/f$ noise was significantly decreased with an Al_2O_3-coated CMOS pore as compared to a SiO_2-coated CMOS pore and a commercially available nitride pore. (d) A lumped element circuit model of a simple nanopore device representing pore resistance, access resistance and membrane capacitance. A more accurate model for the CMOS nanopore chip is superimposed on the geometrical structure of the chip. The displacement current paths between the ionic reservoirs as indicated by 1–4 contribute to the total capacitance of the device.

by the lack of anion selectivity of our pores, as shown in figure 7(b), indicating minimal surface charge effects. Hence the effect of surface charges is neglected in these models and the pore conductance exhibits bulk behavior.

Figure 7(a) shows the pore conductance versus diameter characteristics at 1 M KCl obtained from ten different CMOS-compatible pores and a CMOS pore of varying diameters (4–40 nm). Blue squares represent the TEM drilled pores whereas green circles indicate pores that are fabricated by EBL. To model the conductance of these pores, L and σ were considered to be 66 nm and 11.3 S m^{-1} (at 22 °C). It was found that the conductance of TEM pores can best be described by the hyperboloid model (figure 7(a), black line). Applying a non-linear regression fit to the experimental data, and assuming a linearly varying asymptotic angle α for the hyperbolic model (supplementary data available at stacks.iop.org/Nano/24/155501/mmedia), an outer diameter of $D \approx d + 30$ nm was extracted for the TEM drilled pores. This value is in line with the previous experimental studies reported on pore shape [27, 28, 31]. Alternatively, an equivalent fit (figure 7(a), orange line) could also be obtained using an end-to-end truncated double-cone (i.e. $L_{\text{eff}} = 0$) pore with an angle of $\alpha \approx 14°$ (supplementary data available at stacks.iop.org/Nano/24/155501/mmedia). Though this model is useful for simple geometrical calculations, the sharp edges do not represent the physical picture accurately compared to the hyperboloid model. On the other hand, the best fit to the conductance of EBL pores was obtained by applying the double-cone model (figure 7(a), red line) with $L_{\text{eff}} \approx 58$ nm and $\alpha \approx 71°$. These extracted values suggest that while describing the EBL nanopores the double-cone model almost transforms to a model which assumes a cylindrical

shape for the pore. This can be explained by the fact that EBL pores are most likely to possess a cylindrical structure since they are defined by the anisotropic ICP etch. The small difference in L and L_{eff} probably resulted from the slight horizontal etch at the pore entrance during the ICP process. We also performed the conductance measurements of a CMOS nanopore with diameter 5 nm × 7 nm at three different KCl concentrations. *I–V* characteristics of this pore are given in figure 7(b). The slight non-linear *I–V* behavior could arise from the asymmetric pore geometry and inhomogeneous surface charge distribution [32, 33]. As expected, the conductance of the pore scales with the increasing concentration of KCl.

In addition, the noise characteristics of on-chip nanopores were studied. In the low-frequency regime (<100 Hz), noise is dominated by flicker noise arising from fluctuations in the pore's ionic conductance [34]. Figure 7(c) shows the power spectrum density of current noise at an applied voltage of 100 mV from two CMOS pores with diameter ∼5 nm. CMOS pore 1 is coated with 30 nm ALD Al_2O_3 whereas CMOS pore 2 is covered with 25 nm ALD Al_2O_3 and 3 nm ALD SiO_2. For comparison, we have also included the noise spectrum measured with a similar-size pore in a commercially available (Norcada) 50 μm × 50 μm SiN_x membrane with thickness 30 nm. Pore 1 shows two to three orders of magnitude improvement in low-frequency $1/f$ noise as compared to the other two pores. It has been noted previously that the mobility fluctuation model, via the Hooge parameter, best describes $1/f$ noise in nanopores [34]. This conclusion was based on experimental evidence that the noise is proportional to the density rather than the square of the density as predicted by the surface trap based number fluctuation model. An alternative view is that surface-state scattering induced mobility fluctuation could also lead to the observed behavior [35]. An ALD coated Al_2O_3 pore shows significantly decreased $1/f$ noise compared to an ALD coated SiO_2 pore and an uncoated SiN_x pore, indicating a substantial reduction in surface charged states. The low surface charge exhibited by these pores substantiated by the bulk conductance and non-rectifying behavior further validates the view that charged surface states are reduced by ALD coated Al_2O_3. Thus the sensitivity of a CMOS integrated nanopore can be significantly enhanced by coating it with Al_2O_3.

At high frequencies (>10 kHz), the dominant noise source is interaction of the amplifier's voltage noise with any parasitic capacitance at the amplifier input, including the capacitance from the nanopore device. Hence it is important to minimize the capacitance of the nanopore chip. The capacitance of the CMOS nanopore chip is measured by employing a virtual lock-in amplifier embedded in Patchmaster software (HEKA Instruments). Most of the surface of our CMOS chip was covered with a thick PDMS gasket, leaving only a small circular area (∼diameter 1 mm) exposed to the electrolyte. As a result, the membrane capacitance was reduced to ∼7.8 pF. We also modeled the capacitance of the CMOS nanopore chip. In its simplest form, a nanopore device is modeled as a pore resistance, R_p, in series with an access resistance, R_a, along with the membrane capacitance, C_m (figure 7(d)). A more accurate model can be developed for the CMOS chip by recognizing different displacement current paths (labeled as 1, 2, 3 and 4 in figure 7(d)) between the ionic reservoirs, and calculating the capacitance due to each path by applying the simple expression for capacitance ($C = \frac{K\varepsilon_0 A}{d}$) to each layer of material on the chip. Then the total capacitance of the device is obtained by adding all parallel capacitances ($C_{\text{Total}} = C_1 + C_2 + C_3 + C_4$) (supplementary data available at stacks.iop.org/Nano/24/155501/mmedia). From this model, the total capacitance computed was ∼6.68 pF. This modeled capacitance shows good agreement with the experimentally measured value. The small discrepancy between the theoretical prediction and the experimental result is probably due to the parasitic capacitance resulting from the capacitive coupling between the electrolyte solution and a small part of the CMOS circuitry exposed to it.

3.2. Translocation of DNA molecules

The functionality of on-chip nanopores is demonstrated by performing the translocation studies of λ-DNA. Unmethylated 48.5 kbp double-stranded λ-DNA (length, $L_{\text{DNA}} \sim 16$ μm) was commercially purchased (New England BioLabs). With a negative potential at the *cis* reservoir, a stable open pore conductance was established through *I–V* sweeps and control current measurements prior to the introduction of DNA molecules. No current blockades were observed in the absence of DNA molecules. The molecules were then added to the *cis* reservoir at a concentration between 100 and 500 ng μl^{-1}. Considering a persistence length, l_p of 50 nm, λ-DNA is expected to adopt a highly coiled conformation at high salt concentration with a radius of gyration, $R_g = \sqrt{2l_pL} \approx 1.33$ μm. Once captured by the pore, DNA molecules stretch and traverse the pore. We detected events indicating the translocation of DNA utilizing the previously described CMOS pore. Figure 8(a) plots the ionic current versus time trace at −400 mV before and after the addition of 48.5 kbp λ-DNA. Both linear and folded events were observed in the trace, which is consistent with the translocation studies reported before [36, 37]. A few typical events are shown in the bottom panel of figure 8(a). Translocation events were defined as those that decreased the open pore current by more than three times the standard deviation of the open pore current. Current depressions with durations less than the electrical response of the system (∼60 μs) were excluded from the analysis. The event parameters, peak conductance blockage ratio $B_r^{\text{peak}} = \frac{\Delta G_{\text{peak}}}{G}$ and dwell time t_d, were calculated by analyzing the recorded current trace. The baseline for the current trace was determined by using a moving average over a 50 ms period. Figure 8(b) shows a scatter plot of B_r^{peak} and t_d of a total of 3215 events, where each point represents a single translocating event. The histogram plots of these parameters are also included in figures 8(c) and (d). The histogram of B_r^{peak} can be fitted by the sum of three Gaussian curves as evidenced by three peaks labeled I, II and III. The truncation

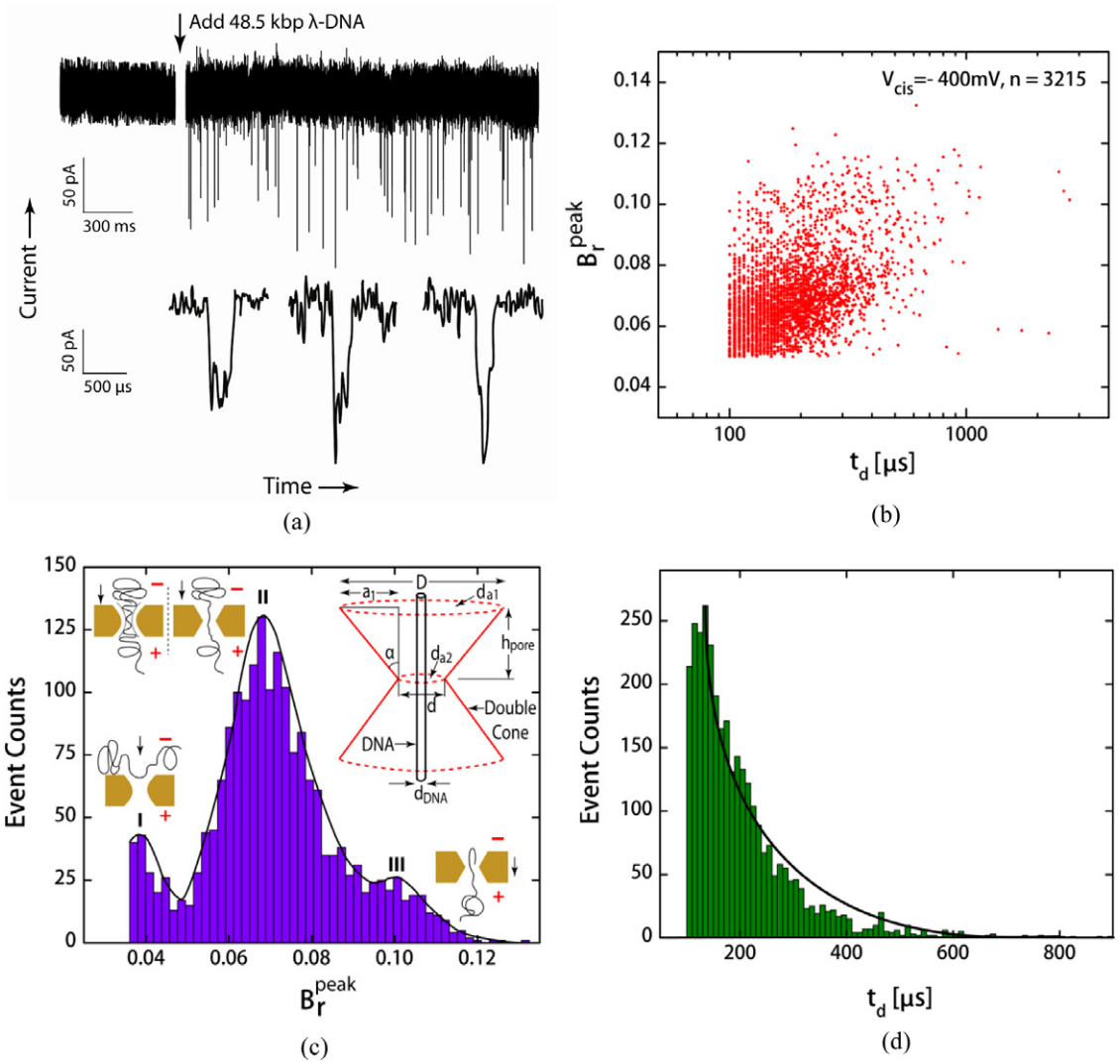

Figure 8. (a) Measured ionic current versus time at −400 mV using a CMOS nanopore with diameter 5 nm × 7 nm. The blockades in the current are due to the translocation of 48.5 kbp λ-DNA molecules. The bottom panel shows three typical events at an increased time resolution. (b) Scatter plot of 3215 events recorded. For each event the dwell time and the peak blockage ratio were determined. Each point in the graph corresponds to a single event. (c) Histogram of observed peak blockage ratio for 48.5 kbp DNA molecules. (d) Histogram of observed dwell times for 48.5 kbp DNA.

of the Gaussian curve I results from the exclusion of events below a threshold value as defined above. We interpret that the Gaussian curves are caused either by the interaction of DNA with the pore or by the presence of single or multiple double strands of the passing DNA inside the pore. Curve I corresponds to shallow blockades indicating interrogation of dsDNA with the pore, curve II represents linear translocation events, and curve III corresponds to deeper blockade events due to single or higher order folding of dsDNA. As seen from figure 8(c), the predominant events are located at a B_r^{peak} value of ∼7%.

To theoretically predict $B_r = \frac{\Delta G}{G}$, we calculated the change in ionic conductance, ΔG through the pore due to the presence of λ-DNA. The hyperboloid model of conductance was employed to determine ΔG since this model provided the best fit to the conductance of TEM nanopores as discussed before. In addition, the DNA molecule was assumed to have a hyperboloid shape. Based on these geometrical considerations, we can obtain ΔG from the following equations [29].

$$\Delta G = G\left(d_{\text{pore}}\right) - G\left(d_{\text{eff}}\right) \tag{2}$$

$$d_{\text{eff}} = \sqrt{d_{\text{pore}}^2 - d_{\text{DNA}}^2} = \sqrt{r_a r_b - d_{\text{DNA}}^2} \tag{3}$$

where d_{pore}, d_{eff} and d_{DNA} are the open pore diameter, the effective pore diameter (with DNA inside the pore) and the thinnest diameter of the hyperboloid dsDNA; r_a and r_b are the major and minor lengths of the elliptical cross-section of the pore. Taking $d_{\text{DNA}} = 2.2$ nm, $r_a = 7$ nm and $r_b = 5$ nm, ΔG calculated from this model was ∼1.33 nS. This yields a blockage ratio of 7.65% (supplementary data available at stacks.iop.org/Nano/24/155501/mmedia). We also obtained a similar result (∼7.14%) for $\overline{B_r}$ by applying the truncated double-cone conductance model with a linear cylindrically shaped DNA inserted coaxially as shown in the top right inset

of figure 8(c). Based on this model, the following expressions were used to calculate B_r.

$$\Delta G = G_{total} - G_{eff} \quad (4)$$

$$G_{eff} = \frac{1}{R_{eff}} = \frac{1}{2 \times (R_{TrCone} + R_a)} \quad (5)$$

$$R_{TrCone} = \frac{4h_{pore}}{\sigma \pi d_{a1} d_{a2}} \quad (6)$$

$$d_{a1} = \sqrt{D^2 - d_{DNA}^2} \quad (7)$$

$$d_{a2} = \sqrt{d^2 - d_{DNA}^2} \quad (8)$$

where d_{a1} and d_{a2} are the effective diameters at the entrance and the narrow part of the cone, h_{pore} is the length of a truncated cone, R_{TrCone} is the effective resistance of a truncated cone and G_{eff} is the total effective conductance of the double cone including access resistance, R_a. Both these models match remarkably well with the experimental value. This indicates that the majority of events are unfolded events. To understand the origin of peak III at ~10% in the histogram, we examined event traces that correspond to this peak blockage ratio. These traces exhibited two distinct levels of blockades, indicating an unfolded strand followed by a folded strand. To model these events, we used the analytically tractable double-cone model with a partially folded cylindrical DNA inside the cone (supplementary data available at stacks.iop.org/Nano/24/155501/mmedia). This model revealed that a B_r^{peak} of ~10% is obtained when the length of the folded part of the DNA inside the double cone, $h_{fold} = h_{pore} \times 98\%$, i.e. approximately half of the pore is occupied by folded DNA. Intuitively, this makes sense, since it would be expected that the small pore diameters used would unravel the DNA at the mouth of the pore. Additionally, the model predicts that events with ~7% blockage ratio are unfolded events. Since the average conductance blockage ratio, $\overline{B_r} = \overline{\frac{\Delta G}{G}}$ obtained from the translocation experiment was also ~7% (supplementary data available at stacks.iop.org/Nano/24/155501/mmedia), the majority of the events are most probably unfolded events, which is atypical of such pores and might be due to the inert surface offered by Al_2O_3 in our pores. The distribution of t_d values is best approximated by a monotonically decreasing exponential function. The average dwell time, $\overline{t_d}$ found from analysis was ~200 μs. Storm *et al* [38] have observed a mean dwell time of ~1 ms for DNA of the same length, under a proportionally smaller voltage bias (120 mV). It has also been shown that dwell times are directly proportional to bias voltage conditions. Applying the above scaling we should observe a $\overline{t_d}$ of ~300 μs, which agrees reasonably well with our results.

4. Conclusions

This work presents the development of nanopore devices in close proximity with the electrodes and amplifier electronics in a foundry fabricated CMOS potentiostat chip implemented in On-Semiconductor's 0.5 μm process. A PIP capacitor was utilized in this process to fabricate oxide membranes containing pores, and polysilicon electrodes. On-chip CMOS circuitry was electrically measured after every fabrication step to confirm that the proposed fabrication process is compatible with CMOS. Nanopores were fabricated in the CMOS process by the combination of TEM drilling and ALD coating. Alternatively, by using EBL and the ALD process, we extended the process to batch fabrication of a large number of nanopore devices on a single CMOS-compatible wafer. However, the diffusion of K^+ ions through the SiO_2 membrane causes high leakage current. This leakage phenomenon was eliminated by coating the membrane with Al_2O_3 which blocks the diffusion of K^+ ions. Al_2O_3 coating of pores also resulted in superior noise performance and increased life-time over other solid-state counterparts. A two to three orders of magnitude improvement in low-frequency noise was observed with Al_2O_3 coated CMOS nanopores as compared to SiO_2 and SiN_x nanopores. A theoretical model for the capacitance of the CMOS nanopore device was also developed by considering different displacement current paths through the device between the ionic reservoirs. The modeled capacitance shows a good match with the low capacitance value experimentally measured with CMOS chips. In addition, the detection of 48.5 kbp λ-DNA using this new architecture was demonstrated with signal-to-noise ratio being on par with the state-of-the-art solid-state nanopore technology. The CMOS integrated nanopore devices described here serve as a platform to implement next-generation nanopore detectors that will offer vastly wider bandwidth and lower noise. Such an integrated approach has the potential to discover new phenomena at the nanoscale governing biomolecule transport and yield a new class of massively parallel biosensors.

5. Methods

5.1. Wafer-scale CMOS-compatible pores by electron beam lithography

The fabrication process started with the deposition of field oxide, polysilicon 1, gate oxide and polysilicon 2 layers on a double side polished 4 in diameter silicon (100) wafer using the process conditions of On-Semiconductor's C5N 0.5 μm technology [10]. 500 nm thick Si_3N_4 passivation layers were deposited on both sides of the wafer by PECVD. An array of 19 × 19 free-standing membranes, spaced 4.6 mm apart, was created in this structure across the wafer following the same process flow as previously described with CMOS chip. The wafer containing membranes was then spin-coated with e-beam resist, ZEP-520A (thickness ~80 nm) and baked on a hotplate at 180 °C for 5 min. EBL was used to pattern circular pores in a JEOL JBX-6300FS system at 100 keV with doses ranging from 5×10^3 to 4×10^5 μC cm^{-2}. Exposed ZEP was developed in 1:1 MIBK:IPA for 60 s and rinsed in 9:1 MIBK:IPA for 30 s at 22 °C. The pattern of pores was then transferred to oxide membranes by ICP etch (CHF_3/O_2 flow rate 45/5 sccm, ICP power 500 W, RF power 100 W, chamber pressure 0.5 Pa, etch time 40 s).

5.2. Atomic layer deposition

Atomic layer deposition of Al_2O_3 was performed in a FlexAL system (Oxford Instruments). Before placement in the ALD system, all samples were exposed to UV/ozone for 10 min to generate reactive hydroxylated surfaces. Trimethylaluminum $[Al(CH_3)_3]$ (Sigma-Aldrich) and O_2 plasma were used as precursor and oxygen source for the film deposition. One reaction cycle of ALD consists of the following steps: (1) flow precursor for 1 s, (2) purge Ar for 5 s, (3) O_2 plasma (RF 150 W) for 5 s and (4) purge Ar for 5 s. The substrate temperature was 300 °C. The deposition rate of Al_2O_3 obtained using this process was 1.15 Å/cycle.

5.3. Nanopore setup

The CMOS chip containing the membrane was horizontally clamped between two acrylic fluidic chambers (figure 5(a)). Poly(dimethylsiloxane) (PDMS) gaskets were used to achieve watertight seal between chip and fluidic compartments. The chip separates two fluidic chambers where the top and bottom chambers contain 80 μl and 15 ml of electrolyte solution. Before placing the chip in the experimental setup, the chip was cleaned in Piranha at 80 °C for 10 min followed by an exposure to O_2 plasma for a minute. This process removes organic contaminants and renders a thin oxide layer on the surface, enhancing the wettability of pores [37]. Immediately after the O_2 exposure, the reservoirs were filled with salt solution, 1 M KCl, 10 mM Tris-HCl buffer, 1 mM EDTA at pH 8. The salt solution was prepared using 18 MΩ Milli-*Q* filtered water (Millipore). Ag/AgCl electrodes were placed in reservoirs for electrical contact to solution. The entire setup was placed in a Faraday cage to minimize electrical noise pick-up. A patch-clamp amplifier and head stage, EPC10 (HEKA Instruments), was used to apply a transmembrane voltage and to detect and amplify the resulting ionic current. The amplified current signal was low-pass filtered at 17.2 kHz using a Bessel filter and digitized at 200 kHz. Data were analyzed using MATLAB (MathWorks) and Clampfit (Axon Instruments).

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