

# Digitally Tunable Optical Power Equalization for Large Port Count Optical Switches

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**Abstract:** A digitally tunable optical power control loop with dynamic range >25dB is designed to compensate losses in large port count multi-stage switch fabrics. At 10 Gb/s with 7.7dBm of input power, the BER is  $6.95 \times 10^{-12}$ .

OCIS codes: (250.3140) Integrated Optoelectronic Circuits; (200.4650) Optical Interconnects

## 1. Introduction

The explosive growth of data traffic within data centers presents a challenge for current electronic network switches to keep up with the demand while meeting power consumption constraints. Optical switching is an attractive alternative that offers high capacity with low power consumption [1]. A large port count switch fabric can be realized by arranging the 2x2 switch elements (SEs) [2-4] in a Crossbar, Benes or Clos variant network topologies. However, crosstalk due to the SE's imperfect extinction ratio and losses in the SE and waveguides limit the number of stages in the fabric. Furthermore, the complexity of driving the SEs electronically grows quickly as the port count increases. The crosstalk issue can be mitigated by adopting network topologies such as the dilated-Benes [5], at the expense of increased number of SE's and slightly higher losses due to the additional number of stages. We propose an electronically assisted integrated photonic switch that alleviates the aforementioned issues. In our approach, we use feedback controlled integrated Semiconductor Optical Amplifiers (SOA) to compensate these losses. The power in the SOA is monitored via built-in detectors (DET). A custom 0.13 $\mu$ m CMOS IC utilizes this output to implement a digitally tunable control loop. Finally, to address the scalability of electronic control to large port counts, we present a novel integration method that enables high density, intimate integration of electronic ICs in photonic ICs.

## 2. Integrated Optical Switch

Traditional Silicon-On-Insulator (SOI) photonic integrated circuits (PIC) with active silicon switches [6] have high fabrication yield, low propagation loss and relatively low switch insertion loss compared to III-V switches. However, the number of switches that can be cascaded to build a larger switch fabric is limited by total insertion loss. SOI PICs do not have an efficient gain element to compensate for the loss. Therefore, to make large port count switch fabric possible, it is advantageous to use a process that contains passive SOI waveguides and interferometers, active silicon PIN injection modulators, and heterogeneously integrated III-V SOAs. The gain characteristics of the SOAs can vary due to process variation, temperature and aging effects. Therefore it is desirable to have the ability to tune each SOA independently through either a one-time calibration, periodic offline calibration or continuously controlled via closed loop feedback. Figure 1 shows the proposed 2x2 Mach-Zehnder Interferometer based SE with active feedback power equalization, fabricated in a wafer-scale hybrid silicon process.

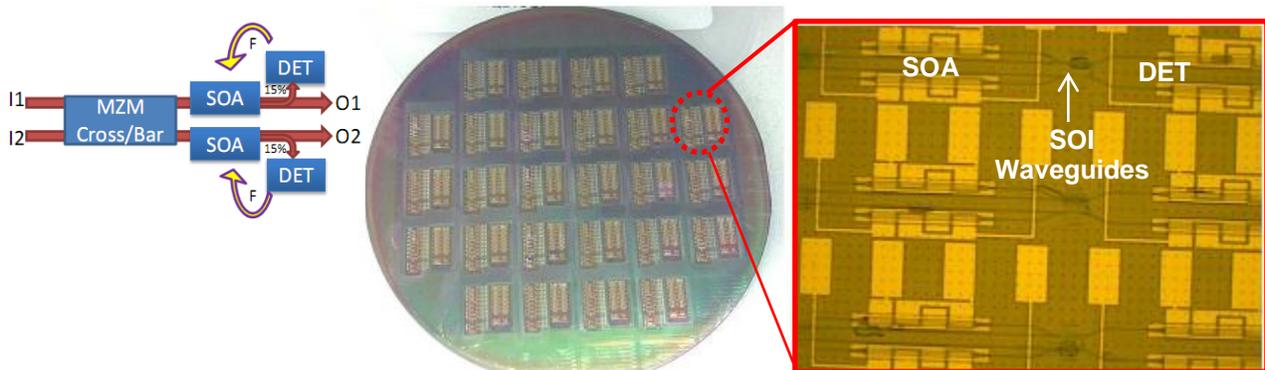


Figure 1. Aurion's 3in diameter wafer-scale hybrid silicon process.

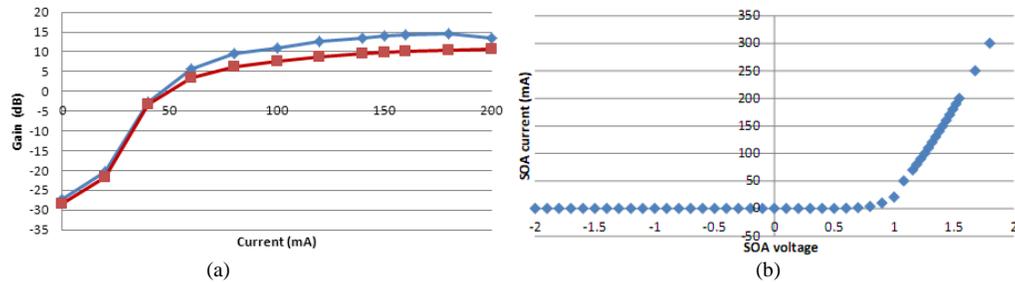


Figure 2. (a) SOA Gain w/input of -4dBm (Blue) and 1.8dBm (Red) at 1550nm vs. bias current at 25°C. (b) I-V Characteristic of the SOA.

### 3. Integration of CMOS IC in PIC

To alleviate the electronic control complexity in a large switch fabric, we developed a process that intimately integrates the EIC with the PIC, which enables short and dense connections between the controller IC and the PIC. In this method PICs are fabricated independent of the EIC. The EIC is integrated in the PIC by etching a cavity in the PIC, placing the CMOS chip in it, planarizing it and establishing metallic contacts. Fig. 3a shows the integration concept where multiple CMOS ICs are integrated in a PIC wafer. Fig. 3b shows a CMOS IC with power detector and SOA driver circuits integrated in the PIC, with metal connections to the PIC's contact pads.

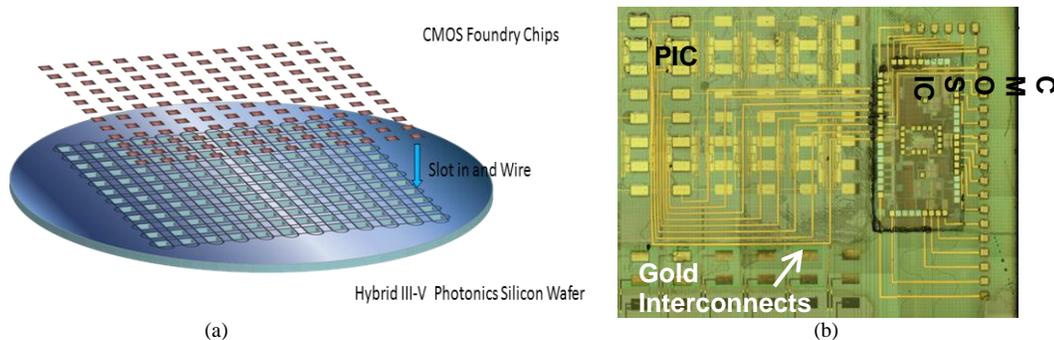


Figure 3. Integration of electronic control IC in PIC.

### 4. Automatic Power Equalization

The power equalization capability is enabled by an on-chip forward biased SOA as the gain element, and a reverse biased SOA as photo detector with an 15% tap to monitor the power. Fig. 2 shows the measured SOA gain at 25 °C using an off-chip 1550nm laser. The photo detector has 60.5nA of dark current, which allows for sensitive measurement of photo current in photo detector mode.

Fig. 4a shows the schematic of the power detector circuit. The power detector is designed to convert an input photocurrent into an oscillating voltage with frequency determined by  $I_{ph}/C_{in}$ . A traditional current-to-voltage transimpedance amplifier's dynamic range is limited by its power supply, which is near 1V in scaled CMOS technologies. By encoding the input amplitude in time, the circuit alleviates the low supply voltage limitation and allows a much wider dynamic range, bounded by the maximum acceptable detection time and maximum oscillation speed of the ring oscillator. The circuit utilizes the photo current from the photo detector as an active load to a NMOS amplifier that is part of a ring oscillator configuration [7]. The slowest rise/fall time effectively controls the oscillation frequency of a ring oscillator. To ensure that the photo current controls the oscillation frequency, we utilize an integrated Metal-Insulator-Metal capacitor to control the rise time due to the photo current. Thus the change due to the photo current is converted into a rising voltage by the integration of charge on the capacitor. This conversion from current to charge effectively encodes the signal in time alleviating the issue due to a limited power supply. The output of the power detector circuit can be read using a frequency counter. Fig. 4a shows the measured detector count versus input power in the photo detector.

Fig. 4b shows the schematic diagram of the driver [8] designed to drive two SOAs in a 2x2 switch. The drivers are binary weighted NMOS transistors that are digitally controlled with 6 bits of resolution each, allowing output currents from 3.3mA to 223mA. The control bits are loaded via a 12-bit serial shift register that operates at clock speed up to 20MHz. A set of D flip-flops isolate the shift register from the driver, preventing rapid switching of the drivers during the configuration phase.

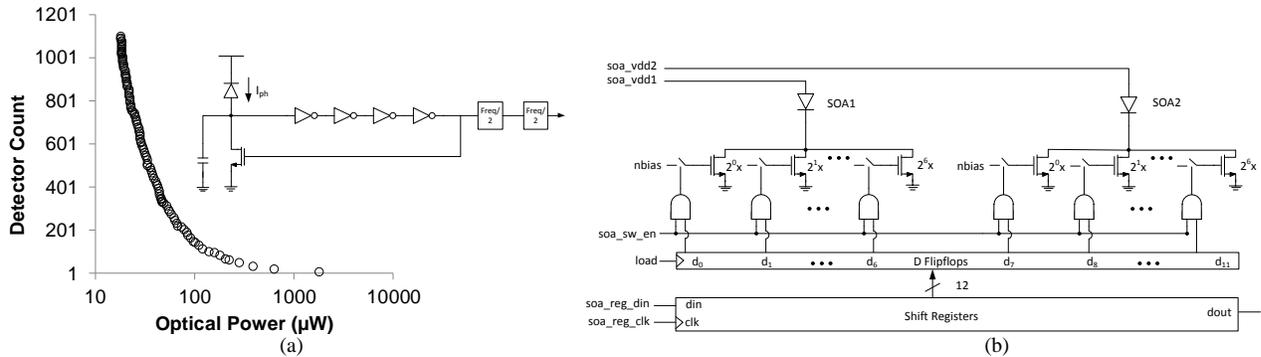


Figure 4. (a) Circuit schematic of the LF-TIA and measured counter response. (b) SOA driver circuit with serial control interface

A Proportional-Integral control loop is setup using Labview and NI USB-6229 Data Acquisition (DAQ). The power detector’s output is read using the built-in 80MHz frequency counter on the DAQ. SOA drive current is established via serial commands produced using the DAQ’s digital output channels. The loop runs at a maximum rate of 1KHz, limited by the Desktop operating system. The control speed can be greatly improved if a real-time Operating System or a Field Programmable Gate Array is used. A test setup to demonstrate the automatic gain control loop operating on modulated data is shown in Fig 5a. A 1550nm laser signal is modulated at 10Gb/s and amplified to 15dBm. The signal is then wavelength filtered and sent through an optical attenuator to vary the input power at the facet of the PIC. The EIC monitors the DET current and adjusts the SOA current to give constant output power. The PIC output signal is amplified, wavelength filtered, and monitored on an Optical Spectrum Analyzer and an oscilloscope. Fig. 5b shows the measured output optical power as function of input power with the control loop turned on. The system regulates the output to about -6dBm, excluding coupling losses on the facets (-16dB). Between 0 to 25.4dBm input, the average output is -6.98dBm with standard deviation of 0.33dB. Fig. 5c shows the output with modulated light with the control loop on. At an input power of 7.7dBm, the measured BER is  $6.95 \times 10^{-12}$ . This approach of using electronics closely integrated with the photonic integrated circuit is important to scaling to large switch sizes because 1) the integration of electronics and photonics allows low power, high impedance drive to the high speed switches and 2) the integration of electronics for a “smart” photonics chip allows drive and bias levels of individual 2x2 switches to be optimized along with maintaining appropriate optical power levels throughout the chip.

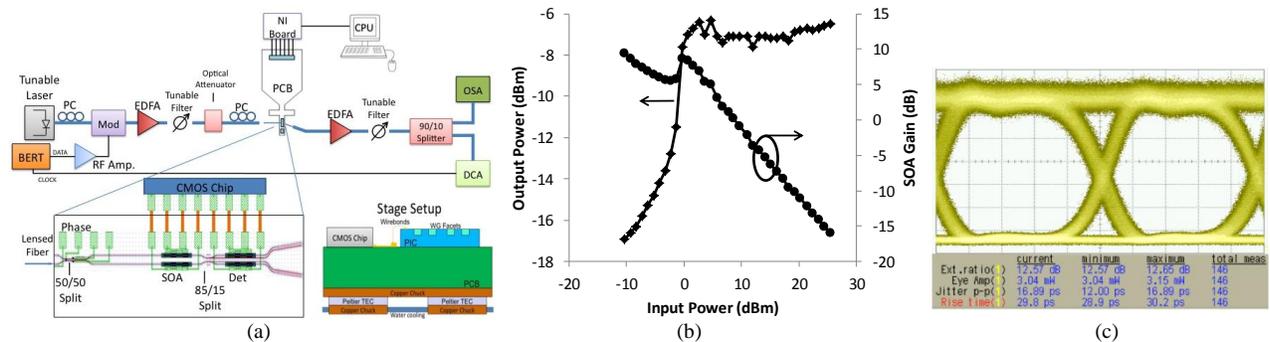


Figure 5. (a) Test setup. (b) Result with automatic power equalization. (c)  $2^{31}-1$  PRBS 10Gb/s eye diagram at 10dBm input power

5. References

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