An 18μW 79dB-DR 20KHz-BW MASH ΔΣ Modulator Utilizing Self-Biased Amplifiers for Biomedical Applications

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Abstract

This paper presents a micro power, area-efficient 4th-order MASH delta-sigma modulator based on a novel self-biased amplifiers for neural sensing applications. A high-gain self-biased CMOS amplifier is proposed to achieve low power operation. Floating correlated double sampling technique is devised to enhance the amplifer's gain-linearity and hence the modulator's SFDR and SNDR performance. Fabricated in a 0.13 μm CMOS process, the prototype achieves 71 dB peak SNDR and 79 dB peak DR over 20 KHz neural signal bandwidth, while occupying only 0.06 mm^2 silicon area. By optimizing the power budgets for different amplifiers, the MASH modulator consumes only 18 μW from 1.5 V supply. The proposed circuit techniques can be applied to other operational transconductance amplifier-based circuits for low power, high speed, and area-efficient design.

I. Introduction

Digital processing in wireless biomedical devices often necessitates the design of low-power, area-efficient and high-precision ΔΣ ADCs. Despite many system innovations to improve the modulator performance, the OTA design in scaled CMOS processes remains the fundamental bottleneck. Several new circuit topologies, such as comparator-based switched capacitor (CBSC) circuits [1], the class-C inverter [2, 3], and the super inverter [4], have been reported to circumvent the limitation of the OTA. Though the CBSC circuit can be utilized to eliminate the use of an OTA [1], it requires a complicated settling process for approximating the closed-loop feedback system. For single-loop ΔΣ modulators, the CMOS inverter-based topology offers many advantages over the OTA [2, 3], but its operation is severely affected by common-mode and power-supply noise. We have recently proposed a self-biased differential amplifier topology [4], which we call the super-inverter amplifier, to mitigate these issues. The drawback is that the positive feedback-loop in the cross-coupled cascode stage degrades the amplifier gain-linearity. Hence, the design of higher resolution architectures, such as the MASH ΔΣ modulator, becomes challenging. This paper presents two strategies to enable the design of MASH architectures based on self-biased amplifiers. One uses a floating correlated double sampling (FCDS) circuit to enhance the gain-linearity of the super inverter, and the other is based on a high-gain SElf-biased cMOS (SEMOS) amplifier.

This paper is organized in the following order. Section II discusses the system condiserations of the MASH modulator. Section III describes the circuit details of the FCDS topology. Section IV analyzes the operation principles of the SEMOS amplifier. Section V presents the measurement results of the fabricated prototype. Section VI concludes the paper.

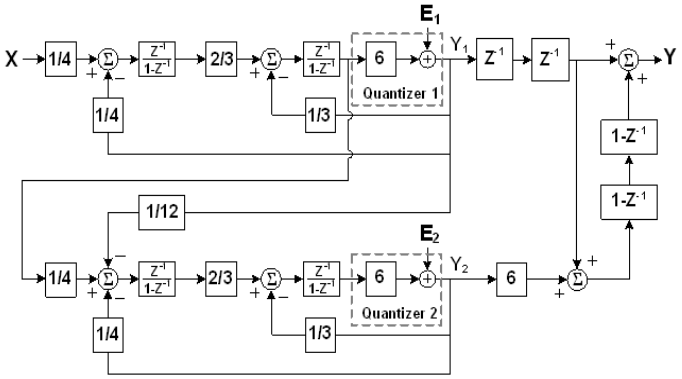

Fig. 1 System diagram of the MASH 2-2 modulator

II. System Considerations

Figure 1 shows the system diagram of the prototyped 4th-order MASH delta-sigma modulator. A 2-2 structure is utilized to relax the filter matching requirements for the second stage. The effectiveness of the MASH modulator relies on two important factors. First, the NTF of the first stage needs to match the digital cancellation filter of the second stage, implying that a high-gain amplifier is used in the first stage. Second, the filter coefficients of the first stage need to be accurately controlled for precisely extracting the quantization noise and this requires a high-speed amplifier. In our MASH prototypes, the FCDS-based design achieves ultra low power and the SEMOS-based design targets reduced clocking complexity at slightly higher power.

III. Floating CDS Circuit

Figure 2 shows the schematic of the FCDS-enhanced 4th-order MASH ΔΣ modulator based on the super inverter (see inset in Figure 3). In the first integrator, two sets of sampling and feedback capacitors are operated in a time-interleaved fashion. Hence, no additional clock phase is required to handle the extra signal processing, and this circuit can run as fast as the conventional SC integrators. During Φ_1, the main path (C_{s1}, C_{f1}) samples the input signal and the secondary path (C_s, C_f)

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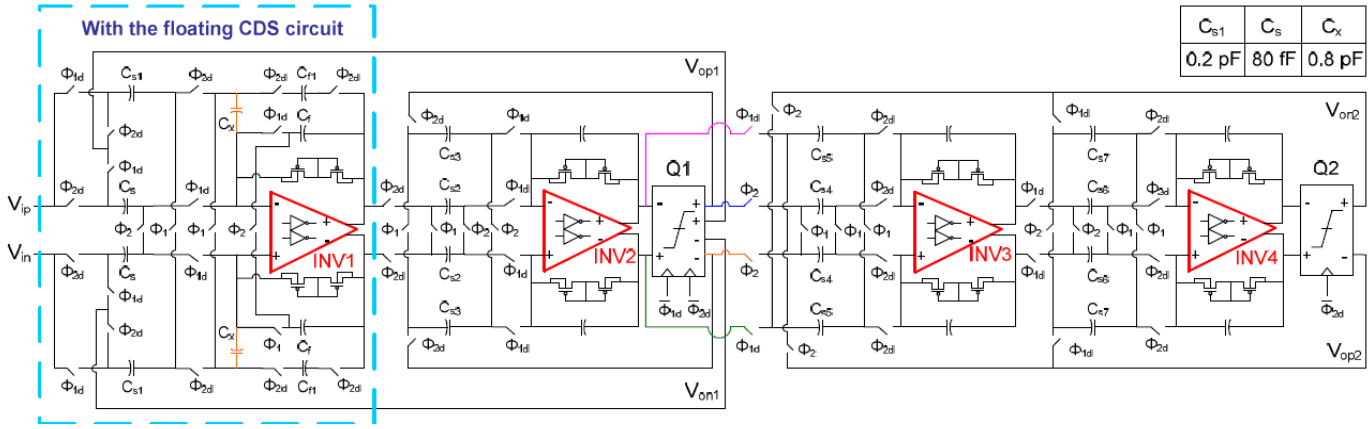

Fig. 2 Circuit schematic of the MASH 2-2 modulator with FCDS enhancement

integrates, while the steady-state error voltage of the super inverter is stored onto the two floating capacitors (C_x). During Φ_2, the two paths exchange roles. The stored voltage on the C_x cancels out the new error voltage of the amplifier to the first order, thereby realizing an accurate virtual ground for the main path. Simultaneously, the output states of the secondary path will be updated by the main path for the error cancellation in the next cycle, thereby enforcing correlation between the two signal paths. Aside from achieving a high DM gain, the amplifier nonlinearity is also mitigated since the FCDS circuit serves as a first order high-pass filter for any input-referred low-frequency errors. The terms "floating" comes from the fact that the CM nodes in the modulator are in high-impedance mode and only differential voltages are processed. This allows for direct DC-coupling without the need for a seperaate on-chip reference. Only the first integrator stage is enhanced with the FCDS circuit since it is the most critical component in the loop filter, which greatly reduces system complexity. Figure 3 illustrates the operation steps of the floating CDS circuit. Pseudo-resistors, formed by two back-to-back diode-connected PMOS devices, are utilized to provide a high-resistance DC feedback path for the integrators. The voltage-dependent nonlinear resistance of the pseudo-resistor also expedites the startup process. The capacitor values are 0.2pF, 80fF, and 0.8pF for C_{s1}, C_s, and C_x, respectively, and the other capacitors are scaled appropriately. For higher power efficiency, the super inverters are also optimally sized according to their locations in the MASH modulator.

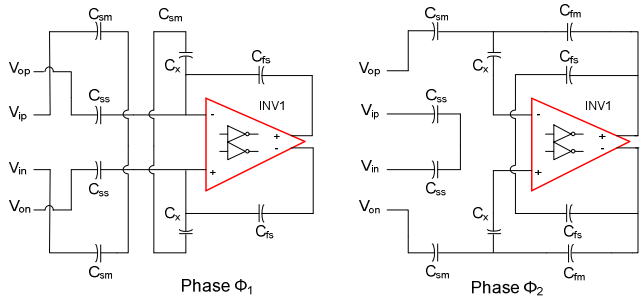

Fig. 3 Operation steps of the FCDS circuit

IV. Self-Biased CMOS Amplifier

In the alternative design, the high-gain SEMOS amplifier is utilized in the first integrator, without the FCDS circuit. The other integrators use the first gain stage of the SEMOS amplifier. The inset in Figure 4 shows the circuit diagram of the SEMOS amplifier. The first gain stage exploits two CMFB circuits ($M_{5,\ 6}$), formed by NMOS and PMOS resistors connected in parallel, to stabilize the DC biasing conditions and suppresses the common-mode (CM) noise from the input and the supply lines. Due to the self-biasing, any nominal DC voltage changes caused by mismatch, process and temperature variations tend to be corrected by the CMFB loops. The bias voltages, the source voltages of transistors M2, provide negative feedback that lowers the bias current in the gain region for differential mode signals. A second stage is added, based on fully differential Bazes amplifier [5], to further increase the gain. Feedforward compensation is utilized to achieve the desired phase margin by directly feeding the input signals to the second stage. No positive feedback loops exist in the two gain stages, and the nonlinear distortion for large output swings mostly results from gain saturation. Designed in a 0.13µm CMOS process, this amplifier achieves 82dB DM gain, 37MHz GBW (with 1pF loads), 63° PM, 98dB CMRR, and 88dB PSRR, while drawing 12µA static current from a 1.5V supply. A detailed discussion of the SEMOS amplifier is given below.

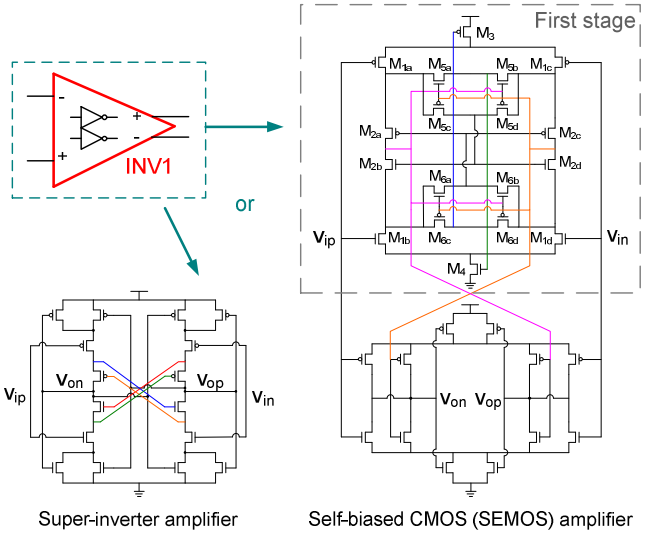

Fig. 4 Circuit diagram of the self-biased amplifiers used in the prototypes

Inverters give lower gain than a biased amplifier due to the fact that the maximum bias current occurs when the inputs are equal due to the complementary nature of the PMOS and NMOS devices. The super inverter circumvents this by utilizing a diod-like feedback from the input to the output and cross-coupled cascode devices for gain enhancement [4]. The SEMOS amplifier on the other hand utilizes an averaging technique of internal voltages to enhance the gain. Figure 5 shows the two transistors $M_{6a,b}$ connected to nodes p_{c1} and p_{c2}. The devices can be safely assumed operating in the linear region due to small drain-source voltages. Since the gates are connected to the differential output voltages the incremental value of the two resistances will be slightly different.

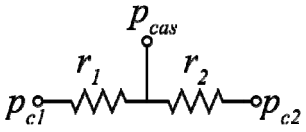

Fig. 5 Simplified model of the bias transistor $M_{6a,b}$

From this simplified model, the cascode PMOS gate voltage can be derived that

$$p_{cas} = p_{c1}\frac{r_2}{r_1+r_2} + p_{c2}\frac{r_1}{r_1+r_2} = p_c + \Delta p_{c1}\frac{r_2/r_1}{1+r_2/r_1} + \Delta p_{c2}\frac{1}{1+r_2/r_1}$$

where p_c is the common mode voltage and can be found by equating the currents in the pmos and nmos stacks. It should also be noted that $p_c \cong n_{cas}$ (cascode NMOS gate voltage) due to the source following action of transistors $M_{2b,d}$. Δp_{c1} and Δp_{c2} are incremental voltage changes around p_c.

$$\Delta p_{c1} \cong \frac{V_{on}}{g_{m6}r_{o6}} + \Delta n_{cas}\frac{g_{m6}r_{in6}}{1+g_{m6}r_{in6}} \cong \frac{V_{on}}{g_{m6}r_{o6}} + \Delta n_{cas} = \frac{-V_{op}}{g_{m6}r_{o6}} + \Delta n_{cas}$$

where r_{in6} is the impedance looking into the source of transistor M_6 and $V_{op} = -V_{on}$ in differential operation. Similarly,

$$\Delta p_{c2} \cong \frac{v_{op}}{g_{m6}r_{o6}} + \Delta n_{cas}$$

Therefore,

$$\Delta p_{cas} = \Delta n_{cas} + \frac{v_{op}}{g_{m6}r_{o6}}\frac{1-r_2/r_1}{1+r_2/r_1} \cong \Delta n_{cas} + g_{m1}r_{o1}v_{ip}\frac{1-r_2/r_1}{1+r_2/r_1}$$

This equation is valid as long as r1 > r2 or if $v_{op} > v_{on}$, else we have

$$\Delta p_{cas} \cong \Delta n_{cas} + g_{m1}r_{o1}v_{in}\frac{r_2/r_1-1}{1+r_2/r_1}$$

The change in n_{cas} voltage, Δn_{cas}, can be derived in a similar fashion. Furthermore, the voltage p_{bias} (blue line) and n_{bias} (green line) have similar dependencies on the input voltages, since they are level shifted version of the input and the resistances involved vary as a higher order function of the input voltage. p_{bias} (or n_{bias}) will fall as the input voltage rise and rise as the input voltage falls constituting the negative feedback loop. This enhances the gain since the current drops in this region. If the input deviations are large, the current will rise temporarily thereby eliminating the slew rate condition. The DC bias condition can be derived by observing that in DC bias conditions, the currents through M_{2a} and M_{2b} have to be equal and also $n_{c1}=n_{c2}=n_{cas}$ and $p_{c1}=p_{c2}=p_{cas}$. Using a simple square law model and ignoring the body-effect, we get

$$I_{bias} = k_p\left(n_{cas} - p_{cas} - |V_{tp}|\right)^2 = k_n\left(p_{cas} - n_{cas} - V_{tn}\right)^2$$

where $k_p=\mu_p C_{os}(W_p/2L_p)$ and $k_p=\mu_p C_{os}(W_n/2L_n)$, then

$$I_{bias} = k_p\left(\frac{\sqrt{k_p}}{\sqrt{k_p}+\sqrt{k_n}}\left(|V_{tp}| - \sqrt{\frac{k_n}{k_p}}V_{tn}\right) - |V_{tp}|\right)^2$$

The above equation only depends on device parameters and hence can be set by appropriate sizing. The bias voltages pbias and nbias can be easily obtained using the following equations, assuming a linear region of operation for M_3 and M_4. A similar equation for p_{bias} can be derived.

$$n_{bias} = \frac{I_{bias}}{2k_nV_{dsn4}} + V_{tn} = \frac{k_p}{2k_nV_{dsn4}}\left(\frac{\sqrt{k_p}}{\sqrt{k_p}+\sqrt{k_n}}\left(|V_{tp}| - \sqrt{\frac{k_n}{k_p}}V_{tn}\right) - |V_{tp}|\right)^2 + V_{tn}$$

If all the device parameters are equal then we can simplify the above equation to

$$n_{bias} = \frac{|V_{tp}|^2}{2V_{dsn4}} + V_{tn}$$

V. Measurement Results

The chip is fabricated in a standard 0.13µm CMOS process with eight metal layers, and each MASH prototype occupies 0.4x0.15mm^2. A microphotograph of the chip is shown in Figure 6. Figure 7 shows the measured 32K-point output power spectrums (overlaid) of the FCDS-based and SEMOS prototypes for a -11dBFS 2KHz sine-wave input. Since the size of input capacitors was chosen to minimize area and power, the in-band noise floor is dominated by the KT/C noise. Figure 8 shows the measured SNR and SNDR versus input amplitude for both MASH prototypes. Compared to the SEMOS-based design, the FCDS method shows better power efficiency and noise performance. Due to increased mismatch between the successive input samples, however, the FCDS efficiency rolls off at large input amplitudes. Figure 9 shows the spectrum comparison of 2nd-order super inverter-based ΔΣ modulators with/without FCDS circuit. It is clear that the FCDS circuit not only lowers the in-band KT/C noise floor by roughly 15dB, but also greatly suppresses harmonic distortions. Table I summarizes the measured performances of both MASH prototypes, where FOM=Power / (2×BW×2^{ENOB}). Figure 10 compares the FOM of this MASH modulator with the other state-of-the-art ADC designs based on an ADC performance survey [6]. Further improvement of the FOM is possible by integrating both the FCDS circuit and the single-stage version of the SEMOS amplifier in the same architecture.

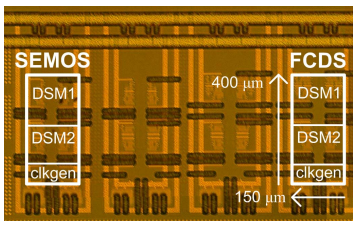

Fig. 6 Chip microphotograph

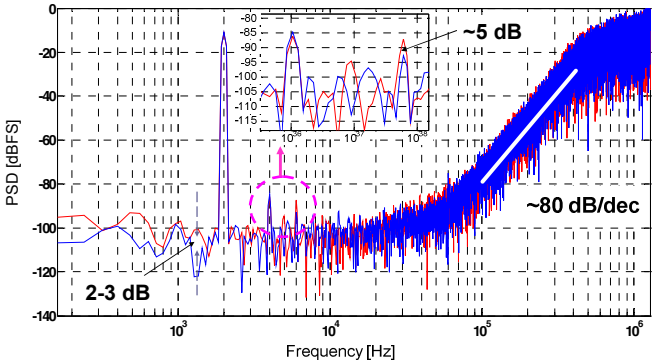

Fig. 7 Measured output spectrums of both the FCDS and SEMOS-based MASH prototypes

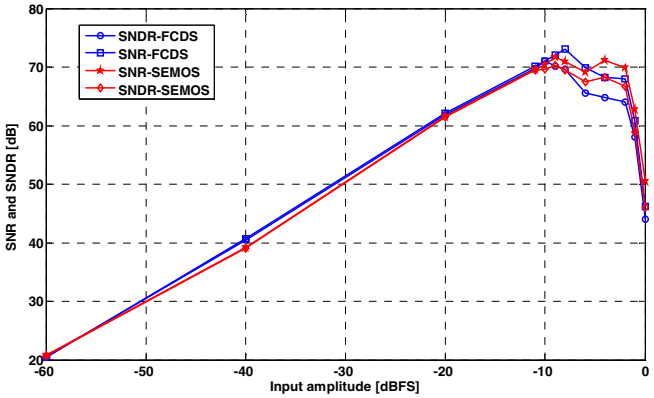

Fig. 8 Measured SNR and SNDR versus input amplitude for both the FCDS and SEMOS-based MASH prototypes

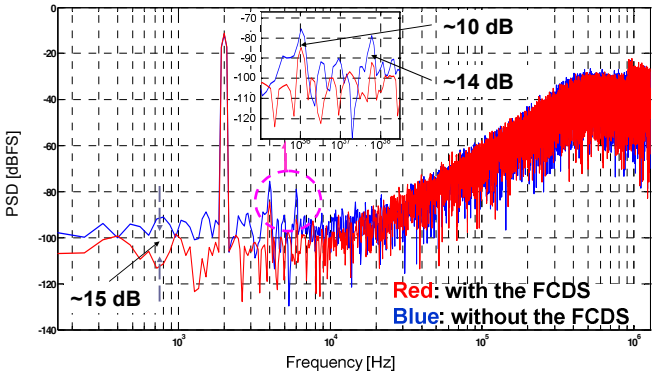

Fig. 9 Measured output spectrums of two 2nd-order super inverter-based ΔΣ modulators with/without the FCDS circuit

TABLE I Performance Summaries

	FCDS	SEMOS
Supply voltage (V)	1.5	
Clock frequency (MHz)	2.56	
Signal bandwidth (KHz)	20	
Peak SNR (dB)	73.2	71.6
Peak SNDR (dB)	71.1	70.2
DR (dB)	79.2	80.6
ENOB (bits)	11.5	11.4
Peak SFDR (dB)	74.6	74.9
Core power consumption* (μW)	18	28
FOM (pJ/conversion-step)	0.15	0.26
Die size/Process	0.4x0.15 mm^2/0.13μm CMOS	

* Excluding the output buffers

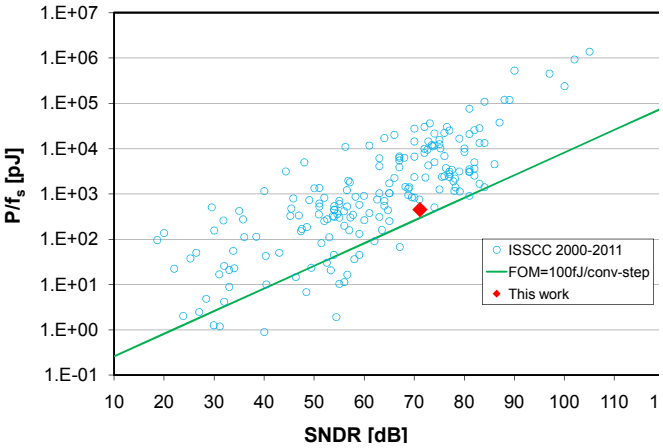

Fig. 10 Performance comparison between the prototyped MASH modulator and the state-of-the-art ADC design

VI. Conclusion

This paper introduces a novel high-gain self-biased CMOS amplifier and a floating correlated double sampling technique to enhance the amplifier's gain-linearity performance. Their application in the design of a prototype 4th-order MASH2-2 modulator is successfully demonstrated. This work not only shows the power efficiency and design robustness of the proposed circuit techniques in developing biomedial devices, but also proves their potential for other lower power, high-speed, and area-efficient SC circuit design in scaled CMOS processes.

Acknowledgement

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