ANALOG VLSI IMPLEMENTATIONS OF RECEPTIVE FIELD PROFILES FOUND IN VISUAL CORTICAL NEURONS

Luke Theogarajan and L. A. Akers
Center for Solid State Electronics Research
Arizona State University
Tempe, AZ
85287-5706
e-mail: lakers@asu.edu

ABSTRACT

Receptive field structures found in the visual cortex of the mammalian brain resemble Gabor filters. There has been recent interest in the use of such receptive field profiles for image coding and texture processing. Systems employing such Gabor filters have been implemented in software for a variety of applications. We believe a hardware implementation of such cells will be helpful in artificial visual processing. We have implemented analog VLSI cells which perform such Gabor-like functions. We describe experimental and simulated results of our circuit. We have implemented both the sine and cosine type of circuits. The sine and cosine circuits described can also be used as edge detection units and on-off center-surround units respectively. Our circuit is the first hardware implementation of a Gabor approximation circuit.

1. INTRODUCTION

Neurons found in the primary visual cortex, i.e. the striate cortex, act as localized spatial frequency filters[1]. The receptive field profiles of such cells resemble even-symmetric or odd-symmetric Gabor filters[1]. There are two classes of orientation-selective cells found in the visual cortex[2]. Cells with two principal subregions, one excitatory and the other inhibitory, and cells with a central on or off region flanked on both sides by an antagonistic surround. The profile of the first class of cells resembles a localized sine wave and the second class a localized cosine wave both localized by a Gaussian-like profile. The first class of cells selectively respond to an edge and the second class responds to bar width. There two schools of thought over the function of the visual cortical neurons. Some researchers believe that the visual cortical neurons act as feature detectors[3], while others believe that cortical neurons act as spatial filters[4][5]. Each view has its own advantages and both views have very strong correlations. A nice argument in favor of feature detection is presented in [6].

In the second section we describe our sine, cosine, and Gabor analog VLSI circuits. In the third section we describe possible applications of our cell. Finally we summary our contribution.

2. ANALOG VLSI IMPLEMENTATIONS

We present our circuit as a model of visual cortical neurons. We have designed these circuits to respond to single points in space which in case of the logon circuits are represented as voltage pairs. We realize that a transformation from space to voltage is necessary. The output of our sine approximation circuit resembles the output of the silicon retina of Mead[7].

2.1. Sine Approximation Circuit

The circuit implementation of a temporal sine wave is well known and is now considered trivial. The same argument does not hold for a sine wave with respect to an independent variable such as an input voltage. There have been two earlier implementations, one using BJTs [8] and the other using MOS transistors[9]. Both the implementations are similar and use the differential current representation. The normalized output results in a sine wave like profile. We have designed a sine approximation circuit. Our circuit closely follows the implementation given in [9].

We have designed the circuit taking many clues from biological systems. In experimentally derived response profiles of the cells in the visual cortex of the cat the sine profile is obtained by subtracting the response of the inhibition cells from the excitation cells[10]. The profile is equivalent to a Gaussian profile which is split at its center. Such a profile can be implemented in analog VLSI in a similar fashion. The generation of a Gaussian profile is done by using the circuit implementation of Delbruck[11] as shown in Fig. 1. The circuit is based on a simple current correlator shown in Fig. 2. For correlating transistors Delbruck defined a parameter S by:

$$S = \frac{(W/L)_{middle}}{(W/L)_{outer}} \qquad (1)$$

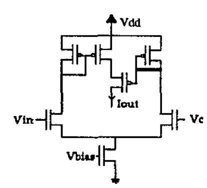

Fig. 1: The bump circuit of Delbruck.

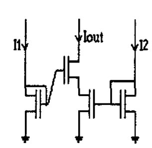

Fig. 2: The simple current correlator.

Assuming the top transistor in the stack is in saturation(subthreshold), the output current of the current correlator can be computed as:

$$I_{out} = S\frac{I_1 I_2}{I_1 + I_2} \qquad (2)$$

If the input currents to the current correlator are the limb currents of a differential amplifier then substituting this in the current correlator relationship provides:

0-7803-3073-0/96/$5.00

$$I_{out} = I_b \frac{S}{4} \operatorname{sech}^2\left(\frac{\kappa \Delta V}{2}\right) \qquad (3)$$

This function gives a bell shaped curve which resembles a Gaussian. We have also reported a circuit that gives a Gaussian profile[12]. However, we will use Delbruck's circuit in the sine implementation because the design allows us to easily generate the sine-like profile. We use our circuit to achieve the Gabor logon profile discussed later.

The output of the circuit in Fig. 1 is fed as a bias current to a differential amplifier. If the input to the differential amplifier is similar to the input of the current correlator then the currents in each limb of the differential amplifier will resemble one half of a Gaussian wave. The input is given by mirroring the current in the input limbs to the limbs of the differential amplifier by means of an additional diode connected transistor as shown in Fig. 3. The circuit implements the following equation:

$$I_{out} = I_b \operatorname{sech}^2\left(\frac{\kappa \Delta V}{2}\right) \tanh\left(\kappa^2 \Delta V\right) + I_{dc} \qquad (4)$$

where $\Delta V = V_1 - V_2$ and I_{dc} is the dc offset current.

The complete circuit diagram is shown in Fig. 3. Transistors m1-m7 form a PMOS version of the bump circuit discussed earlier. Vc determines the zero crossing of the sine circuit. Vbias is the bias voltage to the circuit. This bias must be sufficiently high in order to supply sufficient current to the diode connected transistors m6-m9. This is necessary to generate sufficient voltage levels to the tanh circuit formed by transistors m10-m13 because the sources of the differential pair transistors m10-m11 are not at ground potential but at some higher voltage. The output from a fabricated chip is shown in Fig 4. The effective of different biasing levels is shown. If the biasing level is slowly increased the bump output becomes more wide, quadratic, and then finally flat. For proper circuit operation the bias voltage needs to be at least a few hundred millivolts above threshold. Transistors m15-m16 set a dc offset to the circuit in order for the circuit to be able to vary in the positive and negative direction. There is evidence in biology that there is a baseline firing rate corresponding to the dc level[13]. The input to these transistors are held at Vdd/2 for proper operation. Transistor m14 converts the voltage representation into a current representation. The circuit output is compared to a sine wave and the output approximates a sine wave to 86% and is shown in Fig. 5.

2.2. Sine Logon circuit

The sine logon is obtained by modulating a sine grating by a bivariate Gaussian. We, however, generate the sine logon profile by modulating the output of a edge detection unit by a Gaussian whose input is orthogonal to the input of the edge detection unit. Both profiles resemble each other. The circuit implementing the sine logon is shown in Fig. 6. The bias of the sine circuit shown in Fig. 3 is replaced by the Gaussian circuit presented in [12] and is shown in Fig. 7. The PMOS and NMOS transistors in series act as complementary current correlators. The drain connected PMOS load serves to keep the circuit in the subthreshold region of operation for a large part of the input and also facilitates the mirroring of the current. For symmetrical operation Vdd is kept at 3V. A more detailed description is given in [12]. The advantages of using this circuit are it supplies higher currents. The need for a higher current occurs because the diode connected transistors m7 and m8 need a sufficient input current to generate voltage ranges which allow the differential amplifier to operate properly. Another advantage is that this circuit can be easily made multi-dimensional as shown in [12]. This allows the input to be a complex feature such as lines. We however show results only from the simple implementation. The bias current effectively controls the amplitude of the sine wave and when modulated by a Gaussian bias current results in a sine logon-like profile. The measured output current from this circuit is shown in Fig. 8.

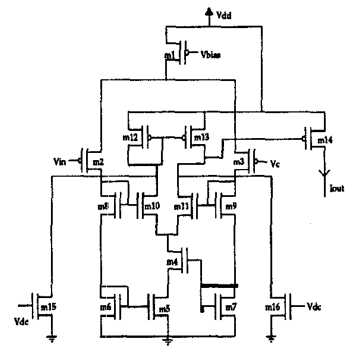

Fig. 3: The sine circuit

2.3. Cosine approximation circuit

A cosine approximation circuit implements an on-center off-surround profile which resembles a Gaussian localized cosine wave. A circuit for generating a cosine wave using BJTs is given in [8]. We, however, use our own implementation using MOS transistors. Our implementation uses fewer number of transistors.

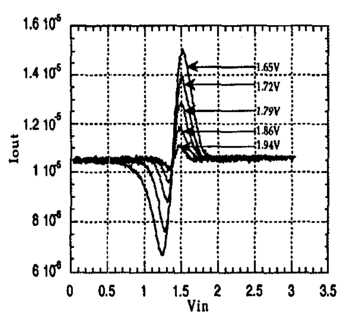

Fig. 4: The measured output currents for different bias voltages to the Sine approximation circuit. Vc was held at 1.4 volts.

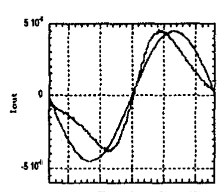

Fig. 5: Comparison of the measured output to a sine wave. The output approximates a sine up to about 86%.

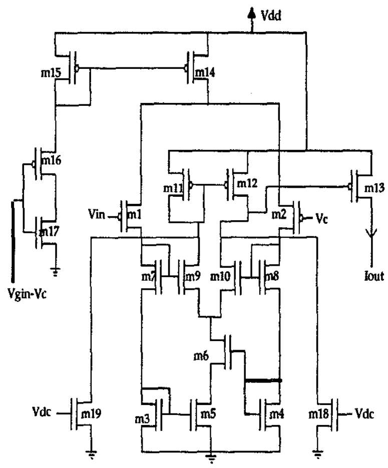

Fig. 6: The Sine Logon approximation circuit.

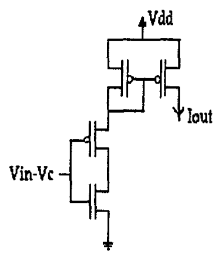

Fig. 7: Our Gaussian cell

Our circuit is shown in Fig. 9. Transistors m1-m7 implement the bump circuit discussed earlier. The output of the bump circuit is fed as a bias current to the differential amplifier. Also the bump circuit output is fed as an input to the differential amplifier. If the other input to the differential amplifier is a voltage that lies in the near the tail of the bump circuit then a cosine like output results. Since we do not know this voltage *a priori* a simple bias will not suffice. We now consider the design of such a bias. Intuitively we know that the peak current occurs when the input to the differential amplifier are equal. Thus if we duplicate this circuit and keeping the inputs equal to the center voltage we can obtain a current that is equal to the current at the peak. But we need the current to be slightly smaller, therefore we have to make the S ratio of the bias circuit slightly smaller than the S ratio of the bump circuit. We used S ratios of .5 for the bump circuit and .48 for the bias circuit. This ratio is calculated assuming equal currents in both limbs to simplify the calculation. This elaborate bias is done to provide robustness to fabrication parameters. Transistors m8-m14 forms the bias circuit, m15, m16, m20 and m21 are the diode connected mirroring transistors. Transistors m17-m19 and m22-m23 form the differential amplifier, m24 converts the voltage to current representation. Transistors m25-m26 forms the dc current bias to the circuit. The output of this circuit is shown in Fig. 10.

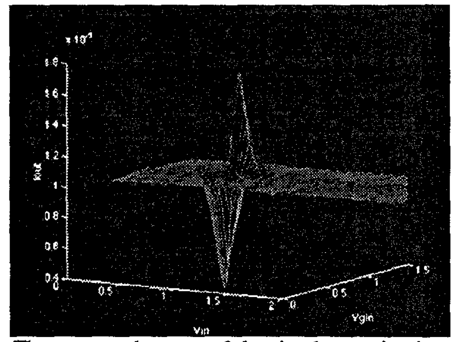

Fig. 8: The measured output of the sine logon circuit.

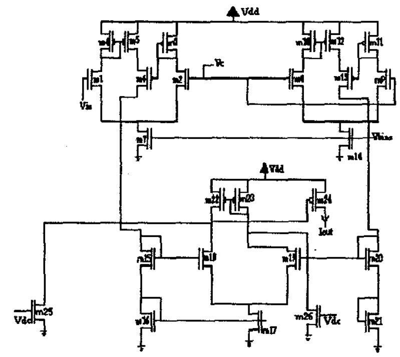

Fig. 9: The Cosine approximation circuit

2.4. Cosine Logon circuit

The cosine logon is designed using the same design philosophy as the sine logon circuit. The complete circuit is shown in Fig. 11. The output of the circuit is shown in Fig. 12.

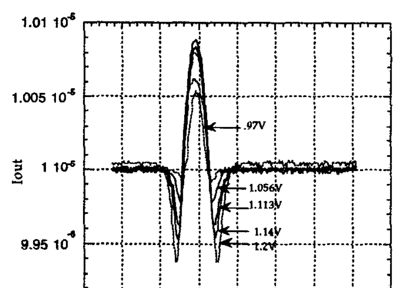

Fig. 10: The measured output of the cosine circuit.

3. APPLICATIONS

The use of Gabor filters in software simulations of visual processing has received a lot of attention lately. Gabor filters present a very efficient coding strategy and have been used widely in image compression[14]. We believe that for real time applications a hardware implementation is necessary. We feel that the above presented circuits fulfill this need. Further, it has been suggested that the spatial information in rats is encoded by phasors[15] i.e. the amplitude and phase of sine wave. Our sine approximation circuit represents an efficient method for implementing this in hardware. Many artificial neural processing systems in hardware employ some form of edge and on or off center units, our sine and cosine circuits are compact implementations of these functions.

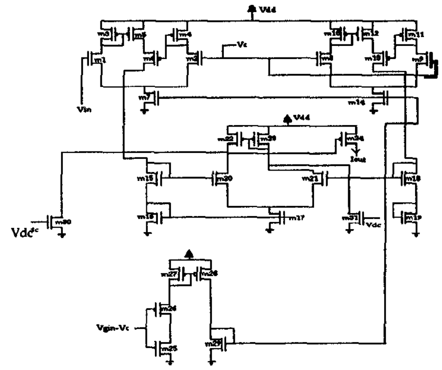

Fig. 11: The Cosine logon Approximation circuit.

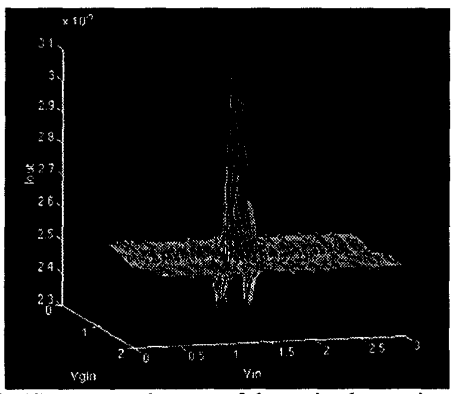

Fig 12. The measured output of the cosine logon circuit.

4. CONCLUSION

Visual cortical neurons perform both as localized spatial frequency filters and simple feature detectors. We have presented compact analog VLSI circuits which perform similar operations. We believe that such cells will be very useful in artificial visual processing. The cells presented may be used as Gabor filters or as simple on-center off-surround cells.

5. REFERENCES

1. D. A. Pollen and S. F. Ronner, "Visual Cortical Neurons as Localized Spatial Frequency Filters", *IEEE Trans. on Systems, Man and Cybernetics*, Sept/Oct 1983.
2. D. H. Hubel and T. N. Wiesel, "Receptive fields, binocular interaction and functional architectures in the cats visual cortex", *Journal of Physiology*, Vol 160, pp. 106-154, 1962
3. P. Mueller, D. Blackman and R. Furman, "Neural Computation of Visual Images", In *An Introduction to Neural and Electronic Networks*, Steven F. Zornetzer, Joel L. Davis, Clifford Lau, editors, Academic Press, 1990.
4. D. A. Pollen, J. R. Lee and J. H. Taylor, "How does the Striate Cortex Begin Reconstruction of the Visual World", *Science*, vol 173, pp. 74-77, July 1971.
5. L. Maffei and A. Fiorentini, "The Visual Cortex as a Spatial Frequency Analyzer", *Vision Research* Vol 13, pp. 1255-1267. Pergamon Press 1973.
6. D. M. MacKay, "Strife over visual cortical function", *Nature*, vol. 289 , pp. 117-118., 15 Jan. 1981
7. C. Mead, Analog VLSI and Neural Systems, *Addison Wesley*, Reading, Mass., 1989.
8. E. Seevinck, Analysis and Synthesis of Translinear Integrated Circuits, *Studies in Electrical and Electronic Engineering*, Elseiver, 1988.
9. R. G. Benson, *Ph.D Thesis*, California Institute of Technology, 1993.
10. J. P. Jones and L. A. Palmer, "An evaluation of the two dimensional Gabor filter model of simple receptive fields in cat striate cortex", *Journal of Neurophysiology*, 18, 229-289, 1987.
11. T. Delbruck, "Bump Circuits", *Caltech Internal Document*, memo 26, 1993.
12. L. Theogarajan and L. A. Akers, "A Multi-dimensional Analog Gaussian Radial Basis Circuit", *Proc. of the International Symposium of Circuits and Systems*, 1996.
13. D. S. Touretzky, A. D. Redish, H. S. Wan, "Neural Representation of Space Using Sinusoidal Arrays", *Neural Computation*, 1993.
14. J. G. Daugman, "Complete discrete 2D Gabor transforms by neural networks for image analysis and compression", *IEEE Trans. on Acoustics, Speech and Signal Processing*, 36, pp. 1169-1178, 1988.
15. J. O'Keefe, "An allocentric spatial model for the hippocamal cognitive map", *Hippocamus* 1(3) pp. 230-235.