An Analog Phase Prediction Based Fractional-N PLL

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***Abstract*— A synthesizer design for achieving high frequency resolution and stability is described. Fractional-N resolution is achieved, without using the classical dual-modulus divider, by exploiting the predictable phase evolution. The predicted phase is added in the feed-forward path within an integer-N analog PLL. A digital pulse generator (DPG) cancels the expected phase difference between the reference and feedback signal. A high-speed current-steering DAC increases the effective pulse width resolution overcoming the limit imposed by the VCO frequency. A novel ping-pong swallow counter topology masks the pipeline delay of a synchronous frequency divider used in the DPG. The architecture has been designed and simulated in a CMOS 0.13 µm technology. For a 5 GHz VCO and 100 MHz reference, the synthesizer exhibits 1.5 Hz frequency steps with the wide-band performance of a conventional charge pump PLL.**

Keywords— Phase-locked loops; Frequency synthesizers; Counting circuits;

I. INTRODUCTION

Frequency synthesisis has seen tremendous advances in the aspect of high-performance, low-cost designs for implementation in mobile communications, IoT devices, and similar transceiver architectures. All-digital PLLs (ADPLLs) allow scalability into lower technology nodes with flexibility and loop configurability for a vast number of RF synthesizer applications [1]. However, abandoning the traditional VCO-based analog PLL limits designs to the frequency resolution and stability that can be achieved with a digitally controlled oscillator (DCO).

Precision RF synthesizers play a role in the recent growth of optical frequency synthesizers, as certain techniques allow RF frequency stability to translate to the optical domain, resulting in relative accuracy of one part in 10^{15} [2], [3]. Higher frequency resolution and stability have allowed numerous applications in the field of optical metrology. This includes observing time variance of fundamental constants [4], measurement of optical frequencies [5], and precision measurements of physics constants [6], [7]. Thus, there is a need for novel PLL architectures capable of frequency synthesis with high precision to enable these applications.

Traditionally, fractional-N synthesizers use a dual modulus divider to achieve high frequency resolution while maintaining the loop bandwidth and settling time offered by integer-N synthesizers. The spurs caused by this quantization noise have been well-studied and converted to out-of-band noise utilizing sigma-delta modulation[8]. Staszewksi et al. introduced an alternative for fractional-N resolution in ADPLLs based on phase prediction in the feed-forward path [1]. The concept utilizes a time-to-digital converter (TDC) to measure the phase difference between the reference and feedback signal, and digitally compare this to the linear ramp expected for fractional synthesis. However, TDC based designs can limit PLL loop bandwidth and therefor are not suitable for servo type applications such as laber stabilization. We present an analog equivalent allowing notable frequency resolution in a single modulus frequency synthesizer.

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The paper is structured as follows: An overview of the system is presented in Section II. Section III describes the novel circuitry designed to realize this architecture at 5 GHz in a 0.13 µm CMOS process. Simulation results and future work are discussed in Section IV.

II. SYSTEM OVERVIEW

The TDC-based ADPLL is shown for reference in Figure 1. TDC quantization error and nonlinearities can contribute to the noise floor and introduce spurs, respectively. This leads to a trade-off between loop bandwidth and in-band phase noise constraints. Recent efforts have increased TDC resolution [9] and calibrated nonlinearities [10] at the cost of complexity, though the ADPLL has yet to match wide-band, low noise performance of a PFD and charge pump. Utilizing a PFD with phase prediction in an analog loop is not as trivial as swapping digital components for analog counterparts.

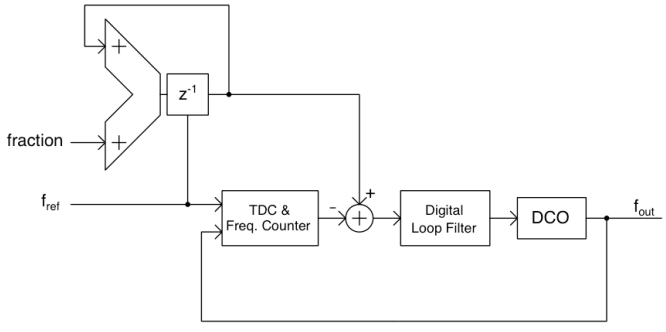

Fig. 1. An ADPLL utilizing a TDC for phase comparison [1]

Consider a traditional integer-N architecture attempting to synthesize a fractional-N frequency. When the feedback signal, f_{OUT}/N, does not equal the reference frequency, f_{REF}, the resultant error signal out of the PFD will be an increasing pulse width that repeats at the beat frequency, $|f_{OUT}/N - f_{REF}|$. The

timing of this is well known for a desired fractional offset and can be cancelled with a complementary signal from a Digital Pulse Generator (DPG), which is defined below and shown in Figure 2.

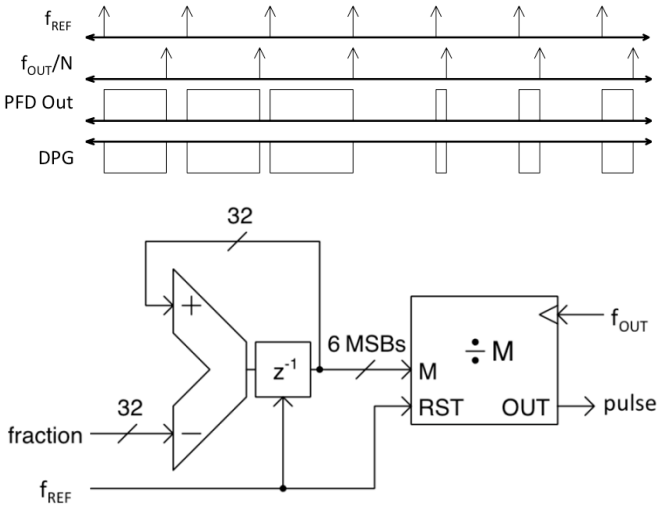

Fig. 2. Digital pulse generator (a) timing diagram and (b) implementation

When the divider M value is close to the integer-N value, there will be a short pulse before the reference signal resets the output. Analogously when M is relatively small, the pulse will be held high for a majority of the period and still reset on f_{REF}, as the system desires. The DPG takes in a 32-bit word that sets the speed of a decumulator whose output MSBs are used to set the M divide word. Resetting to N every time the decumulator reaches 0 creates the required signal pattern with a beat frequency controlled by the fraction word. The design of a 32-bit decumulator at reference clock speeds is relatively straight forward, while the added benefit is a frequency resolution of $f_{REF}/2^{26}$. For our simulated design of f_{OUT} = 5 GHz and f_{REF} = 100 MHz, this translates to 1.5 Hz frequency step resolution at the output.

While the beat frequency can achieve high resolution, the DPG pulse width resolution is limited by the clock period of the VCO. Consider the following example of generating an ideal 1 kHz beat frequency. The PFD output pulse width would slowly increase over 100,000 cycles, 0.1 ps each comparison iteration. However, using a 5 GHz output clock, the DPG can only achieve 200 ps resolution, leading to maximum quantization error of +/- 100 ps. The loop adjusts to account for this quantization error but an inband spur is introduced. In the charge-pump based PLL, these pulses are integrated onto a capacitor to form the tune voltage for the VCO.

Because the quantization error ends up as a delta charge on a cap, we realized it can be cancelled each cycle by adding an opposing current such that the net charge is zero. Though we cannot create a cancellation pulse faster than our output clock, the novel addition of a DAC at the charge pump output allowed us to achieve a shorter effective pulse width.

$$\Delta V_{QE} = \frac{I_{CP} \times t_{QE} - I_{DAC} \times t_{cancel}}{C} \quad (1)$$

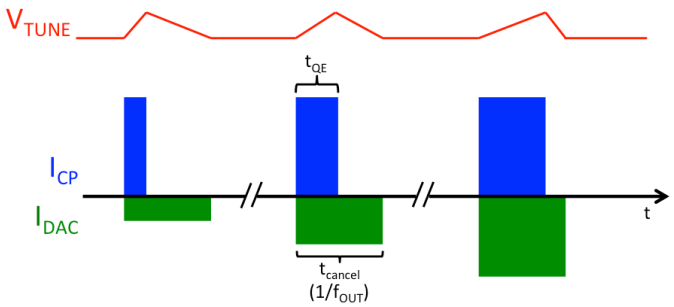

Fig. 3. Illustration of the pulse width quantization error getting cancelled by a pulsed current DAC

A 5-bit DAC with a full scale range equal to the charge pump current was utilized in this design. For a cancellation pulse width of 1 f_{OUT} cycle, this yields an effective resolution of 200 ps / 2^5 and a maximum quantization error of +/- 3.1 ps. Figure 4 shows the full PLL schematic with the addition of the DAC. Notably, the next 5 MSBs from the decumulator inherently form the ideal word for cancellation due to the linear ramp in pulse width quantization error.

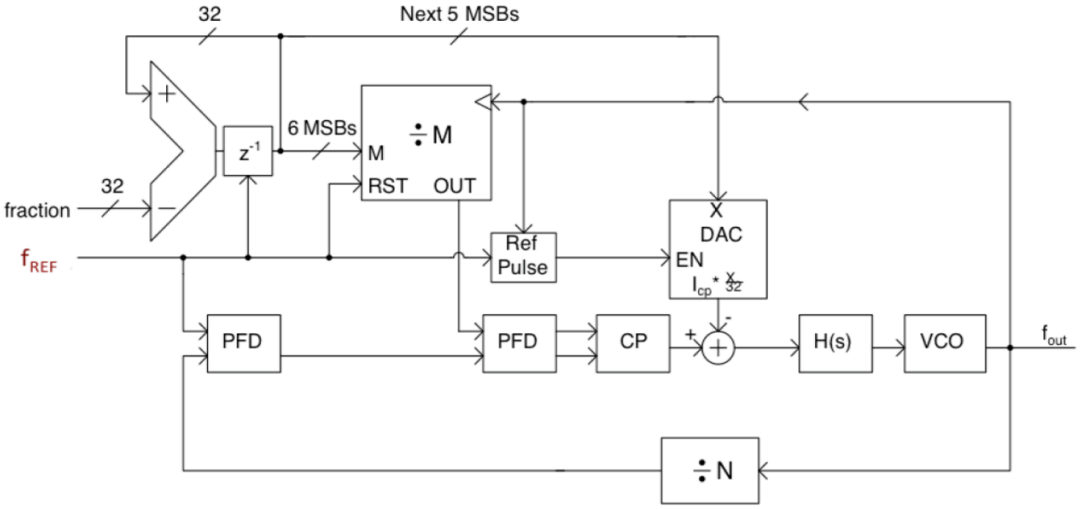

Fig. 4. Analog Phase Prediction based Fractional-N PLL

III. Circuit Implementation

A VCO with a low K_{VCO} (Hz/V) was essential to obtain and measure the frequency resolution this architecture can achieve, without being limited by the expected voltage noise on the VCO control voltage, V_{TUNE}. The differential delay cell design shown below offers a frequency fine-tuning bias that can reduce the amount of current available for switching the inverters[11]. The three-stage implementation demonstrates 4.7-5.1 GHz frequency range with a K_{VCO} of 266 MHz/V.

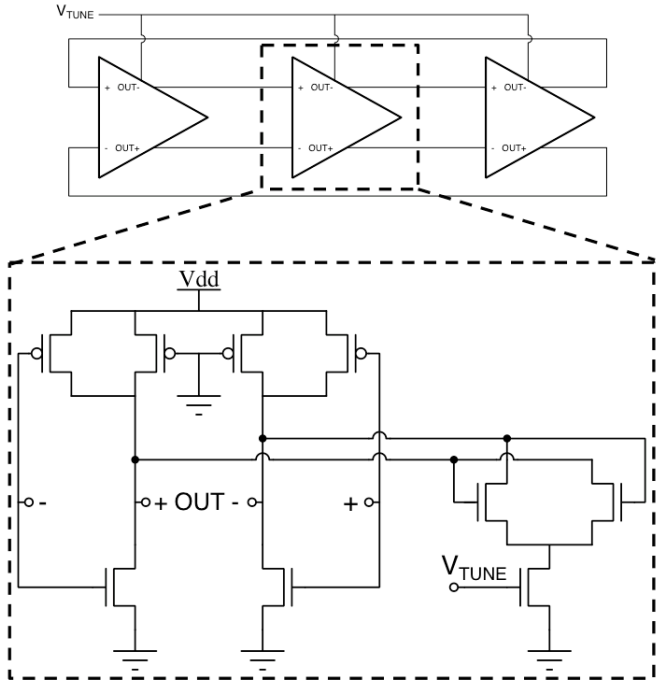

Fig. 5. Differential ring voltage-controlled oscillator

A swallow counter was chosen for the frequency divider to minimize the number of gates switching at the clock frequency. At high-speeds, the combinational logic following the clock dividers presents a significant propagation delay which is divide-word dependent. To maintain a synchronized system, the entire swallow counter was pipelined, with flip-flops following each divide-by-2 and binary comparison. True Single Phase Clock (TSPC) flip-flops were utilized to handle the 5 GHz timing requirements in this technology.

While the pipelined swallow counter is synchronized, it presents a minimum delay path of 9 input clock cycles. For the divide-by-N feedback route, this does not present a problem; the input word is just given as N+9, with a minimum division of 10. The divide-by-M in the DPG however must be able to cover its full range for minimum to maximum duty cycle generation. We solved this by designing a novel ping-pong swallow counter. Delaying the reset signal by 9 cycles through shift registers allowed the minimum divide ratio to return to 1, but the next division would need to start while the previous pipeline is being flushed. To solve this, a second copy of the swallow counter was added to begin the subsequent division while the first is completing. Basic logic is used to toggle between the two dividers at the input and output. The topology is shown in Figure 6.

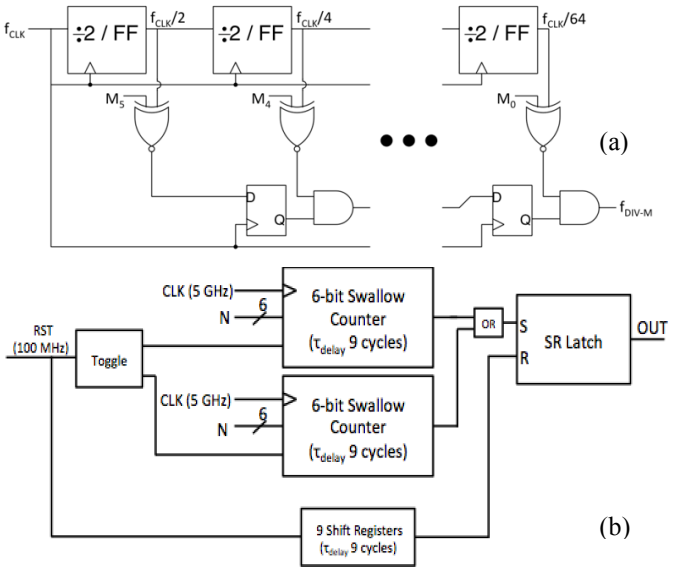

Fig. 6. Design of the (a) pipelined swallow counter and the (b) ping-pong swallow counter topology

Generating 200 ps current pulses requires sources with minimal rise / fall times. A current-steering scheme keeps the bias transistors operating at all times for quicker turn-on at the cost of static power dissipation[12]. A voltage buffer is used to provide a copy of the output voltage on the dummy path side. This prevented current variation between the two paths that would have shown up as a frequency dependent nonuniformity in response time. A servo-loop matches the sink and source currents across the output voltage range by adjusting the bias voltage The DAC, shown in Figure 7, is a replica design of the charge pump but with magnitude variation implemented by switching the cascode node between cut-off and the bias voltage.

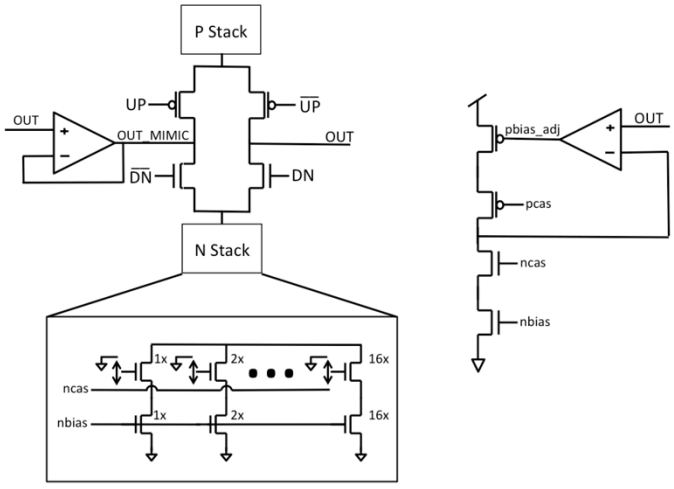

Fig. 7. Current-steering DAC topology

IV. Results and Discussion

Successful frequency synthesis is observed in the transient simulation as shown in Figure 8. The system is started in integer-N mode and switched to fractional-N. System lock is most easily seen in the VCO tune voltage, which first settles at

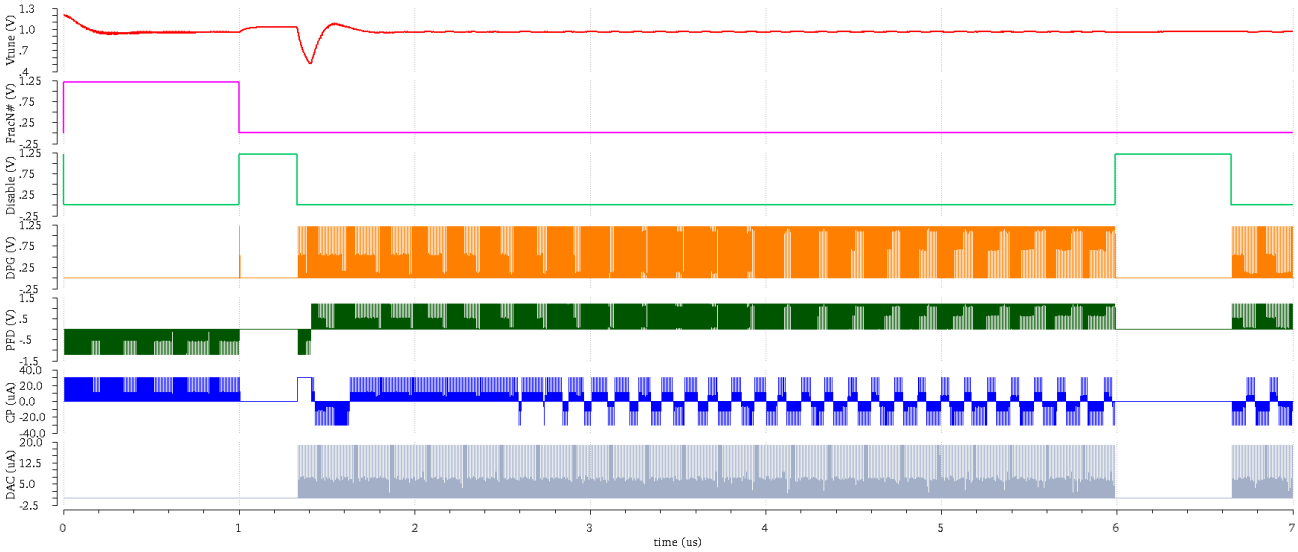

Fig. 8. Transient simulation demonstrating lock of the fractional-N synthesizer

500 ns in integer mode. The 'FractN#' signal transitions to active low at 1 µs, which turns on the DPG and DAC. As expected, the VCO tune voltage adjusts so that the output frequency creates a linear ramp of phase error at the rate of the fractional word. The loop bandwidth of the PLL is 5 MHz.

Early results showed that a slight phase error near the 2π rollover could cause an unwarranted, significant system response. If the DPG has a small duty cycle after completing 2π phase shift while the beat between f_{REF} and f_{OUT}/N has yet to cross 2π, this will result in a significant phase error in the wrong direction. Since the timing of this occurence is inherently known, the simplest solution is to open the loop briefly while the beat frequency goes from high-to-low pulse width. The DPG generates this disable signal which places the charge-pump and DAC in tri–state when asserted.

An improvement for future designs would involve locking to the rising edge of the reference clock while there is π/2 to 3π/2 phase offset from the reference, and locking to the falling edge for 3π/2 to π/2. This would prevent the PFD output from ever reaching the rollover problems described above as the desired duty cycle would always be 25-75%. Additionally, the spur associated with the limited pulse width resolution needs to be eliminated. While an N-bit DAC offers 2^N resolution improvement, a ΣΔ modulation on the DAC could push the quantization noise out of band.

In conclusion, we have presented an architecture utilizing phase prediction in an analog integer-N PLL to achieve fractional-N performance while preserving high loop bandwidths required for servo applications such as laser stabilization.

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